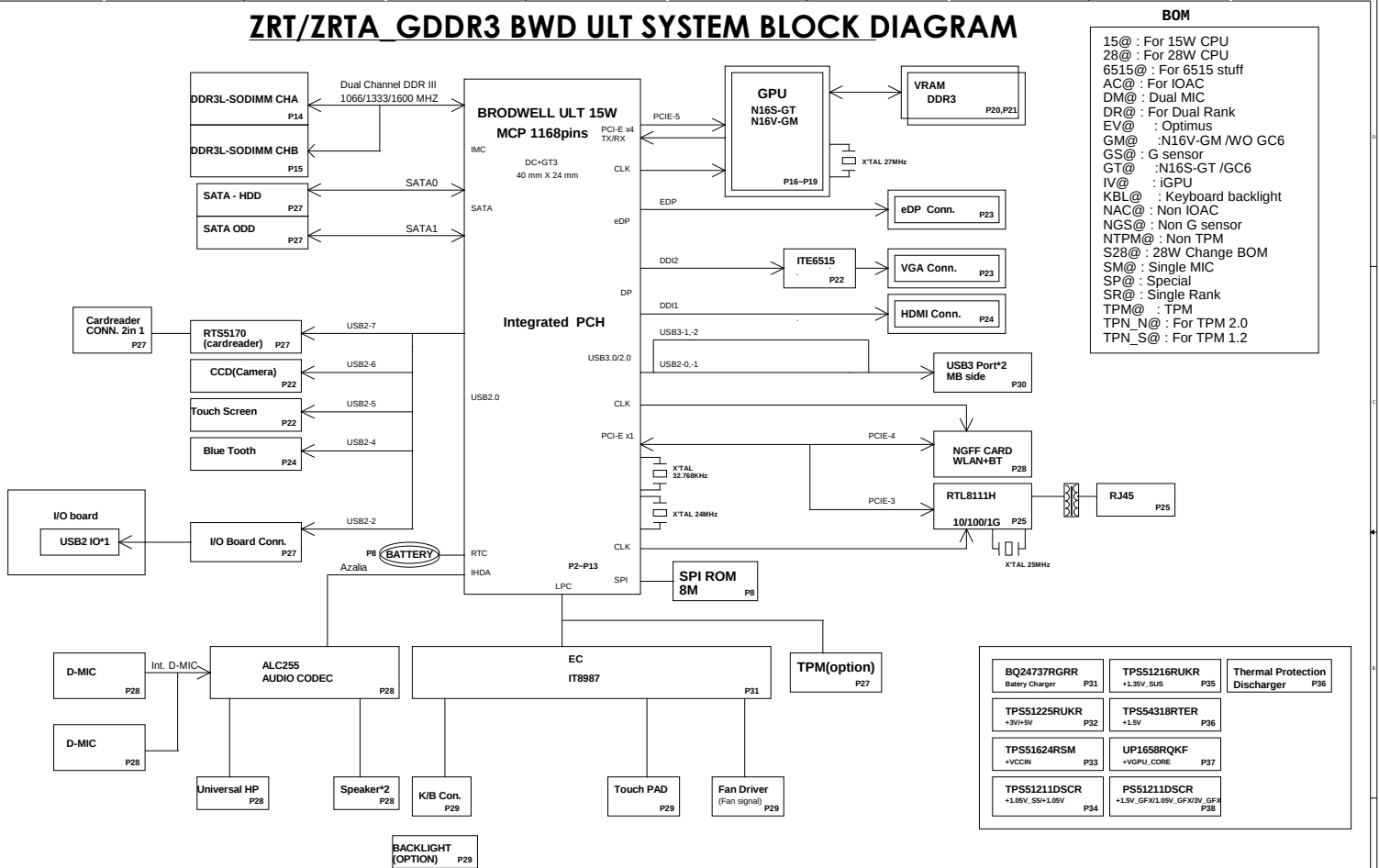
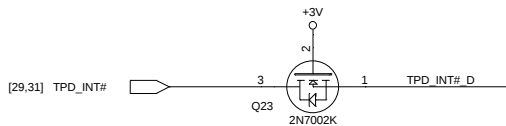
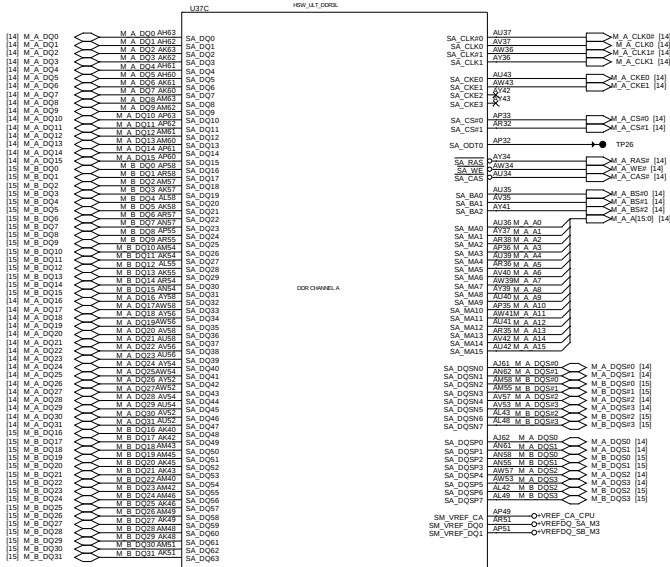


ZRT/ZRTA_GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM



[illegible]

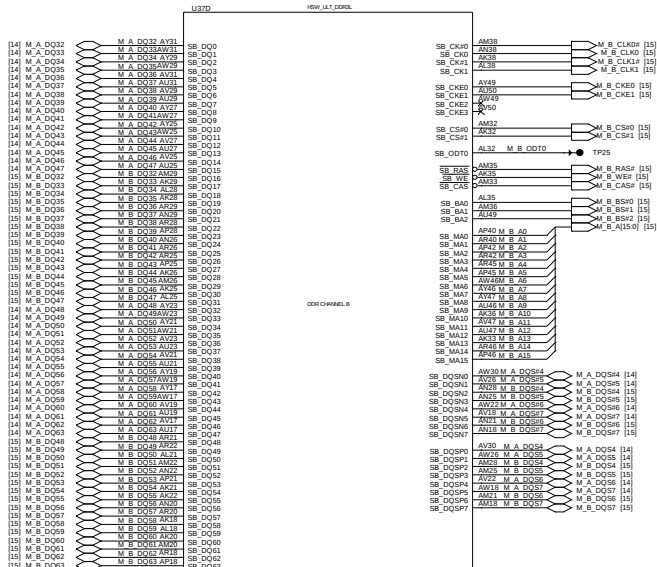
Haswell ULT (DDR3L)



DDR CHANNEL A

3 OF 19

Haswell Processor (DDR3)



DDR CHANNEL B

4 OF 19

Haswell ULT (SIDE BAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >10 mils
Trace Length: 0.4-6.125 inches

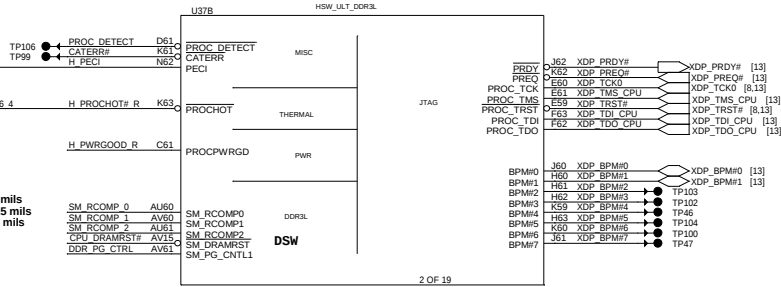
H_PWRGOOD (50ohm)
Trace Length: 1-11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10-17 inches

[31] H_PECI

[31,32,36] H_PROCHOT#

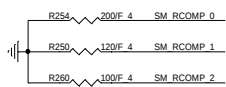
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12-15 mils
Trace spacing = 20 mils



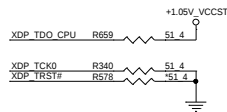
TCK,TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1-6 inches
Length match < 300 mils

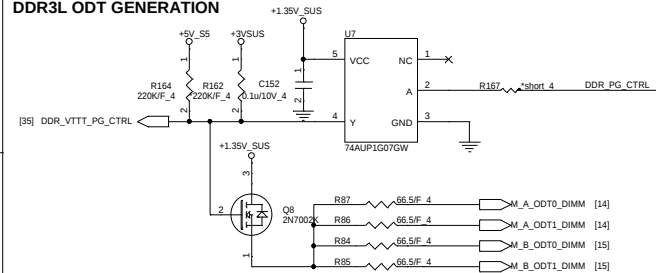
DRAM COMP



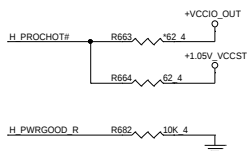
XDP PU/PD



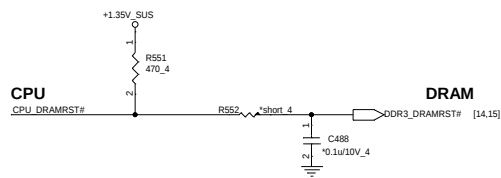
DDR3L ODT GENERATION



PU/PD of CPU

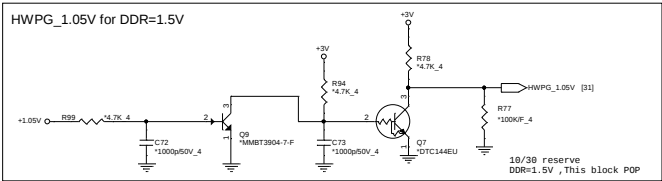
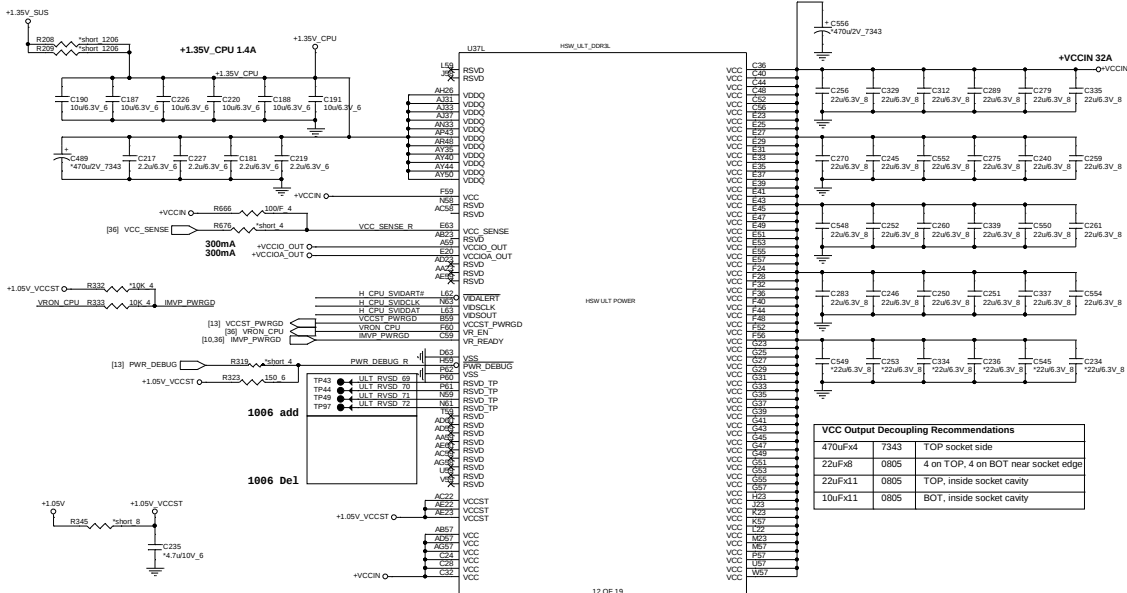


DRAMRST

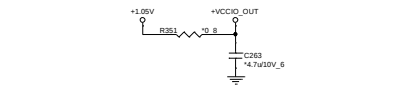
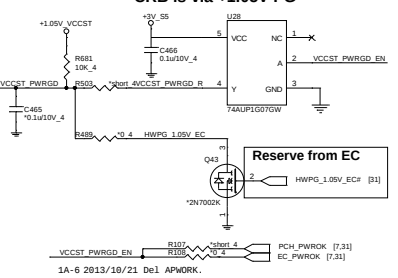


VDDQ Output Decoupling Recommendations			
330uFx2	7343	BOT socket side	
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity	
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity	

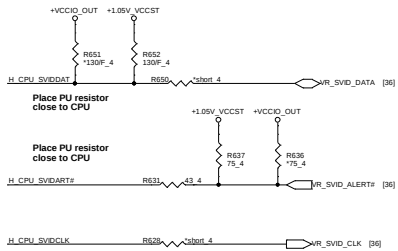
Haswell ULT (POWER)



VCCST PWRGD CRB is via +1.05V PG



SVID Layout note: need routing together and ALERT need between CLK and DATA.



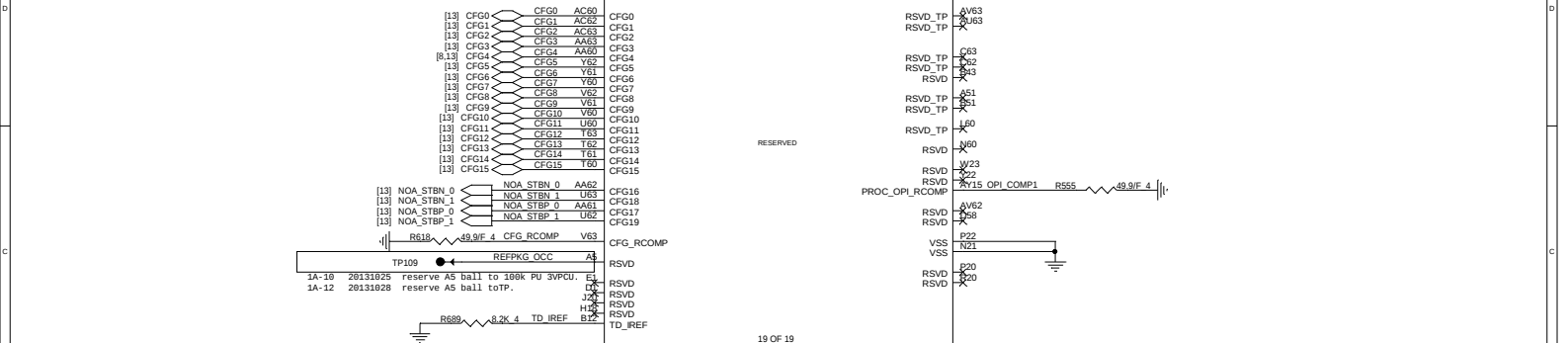


Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Haswell 4/5 (POWER)	3A
Date	Wednesday, February 11, 2015	Printed: 5 of 44

5	4	3	2	1
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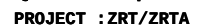


Processor Strapping

CFG000000 - Overlapping		1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL		
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE		
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT		
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT		
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY		
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED		

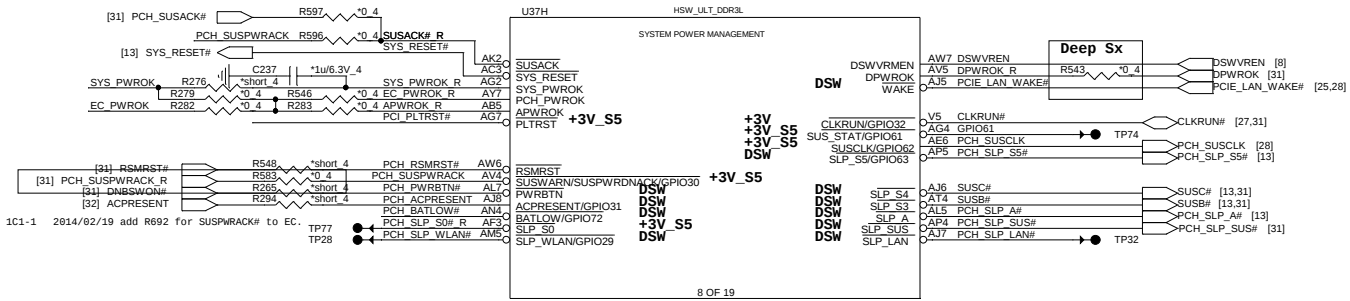
Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A
Date:	Wednesday, February 11, 2015	Sheet 6 of 44

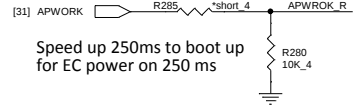
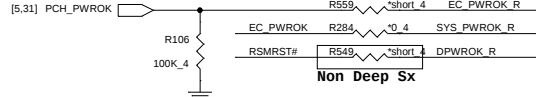


				Size	Document Number	Rev
					Haswell 5/5 (CFG/GND)	3A
				Date:	Wednesday, February 11, 2015	Sheet 6 of 44

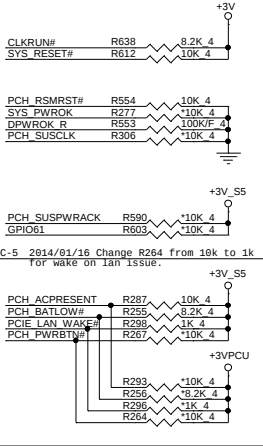
Haswell ULT PM (PM)



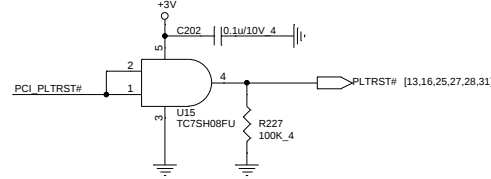
Power Sequence



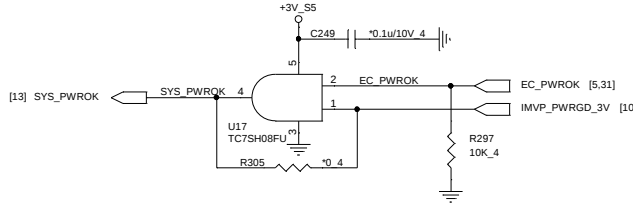
PCH PM PU/PD



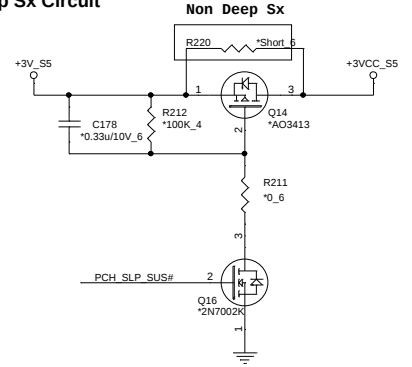
PLTRST# Buffer



SYSPWOK

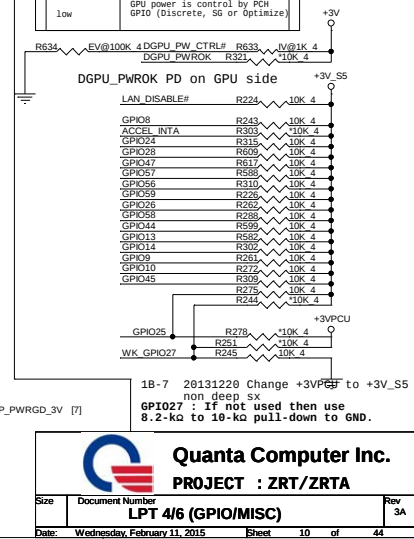
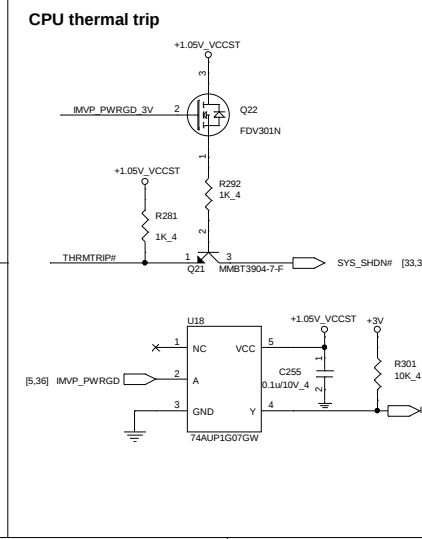
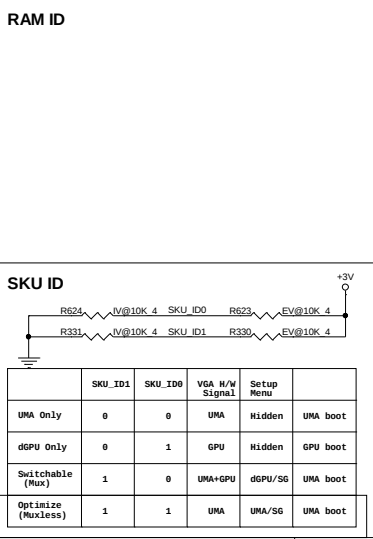
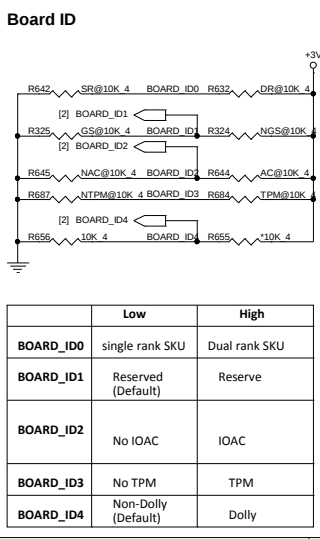
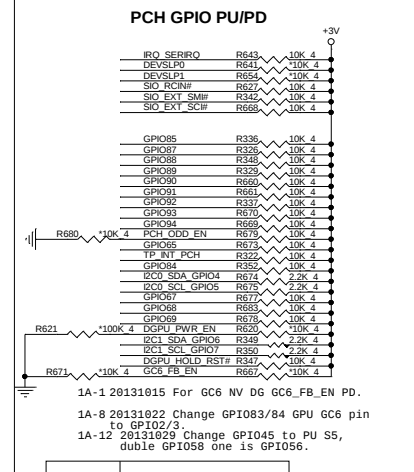
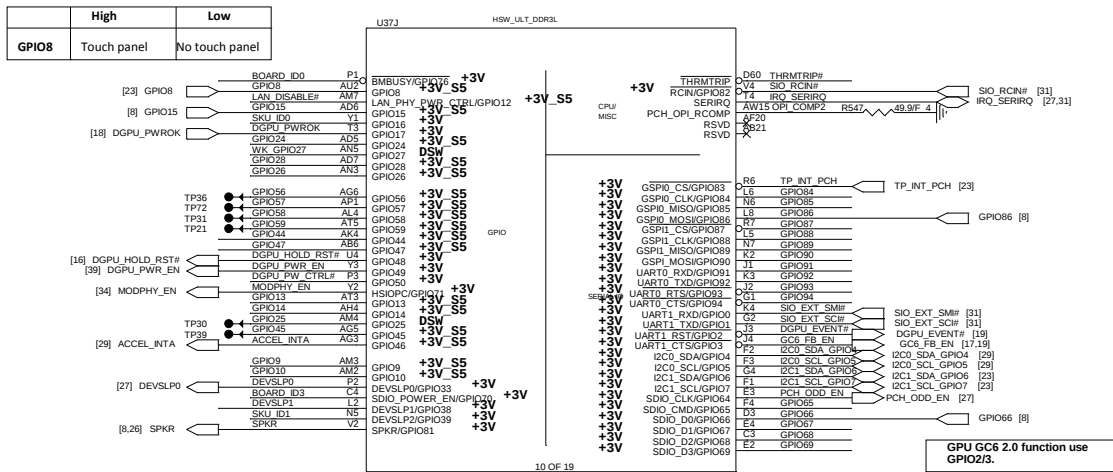


Deep Sx Circuit

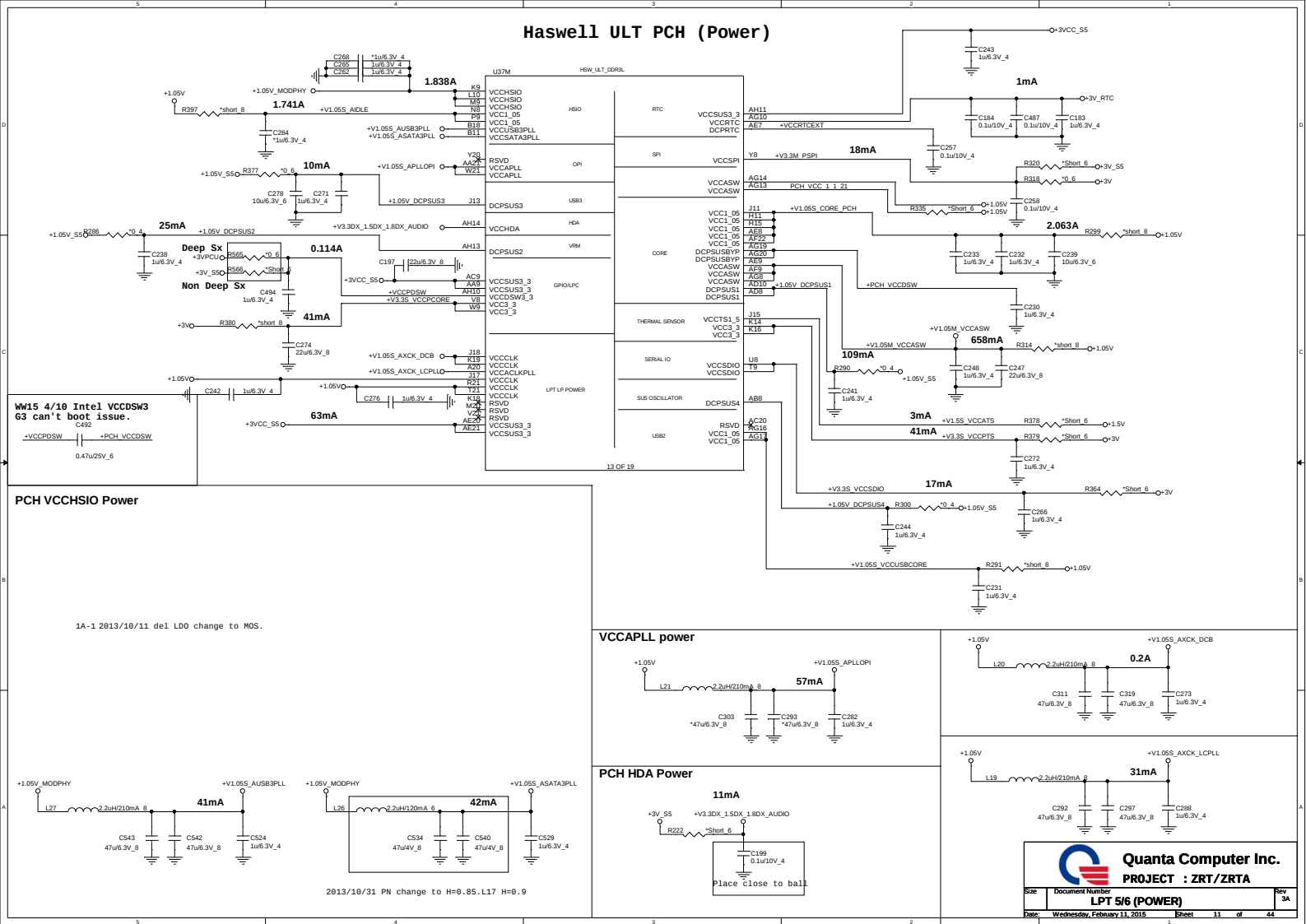


PROJECT : ZRT/ZRTA			
Size	Document Number	LPT 1/6 (DMI/FDI/VGA)	Rev 3A
Date:	Wednesday, February 11, 2015	Sheet 7 of 44	

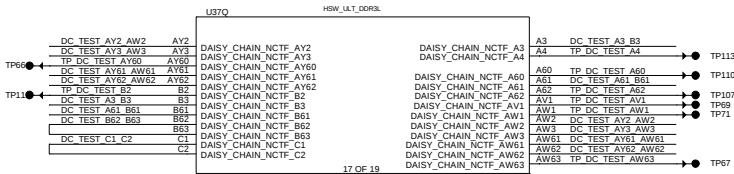
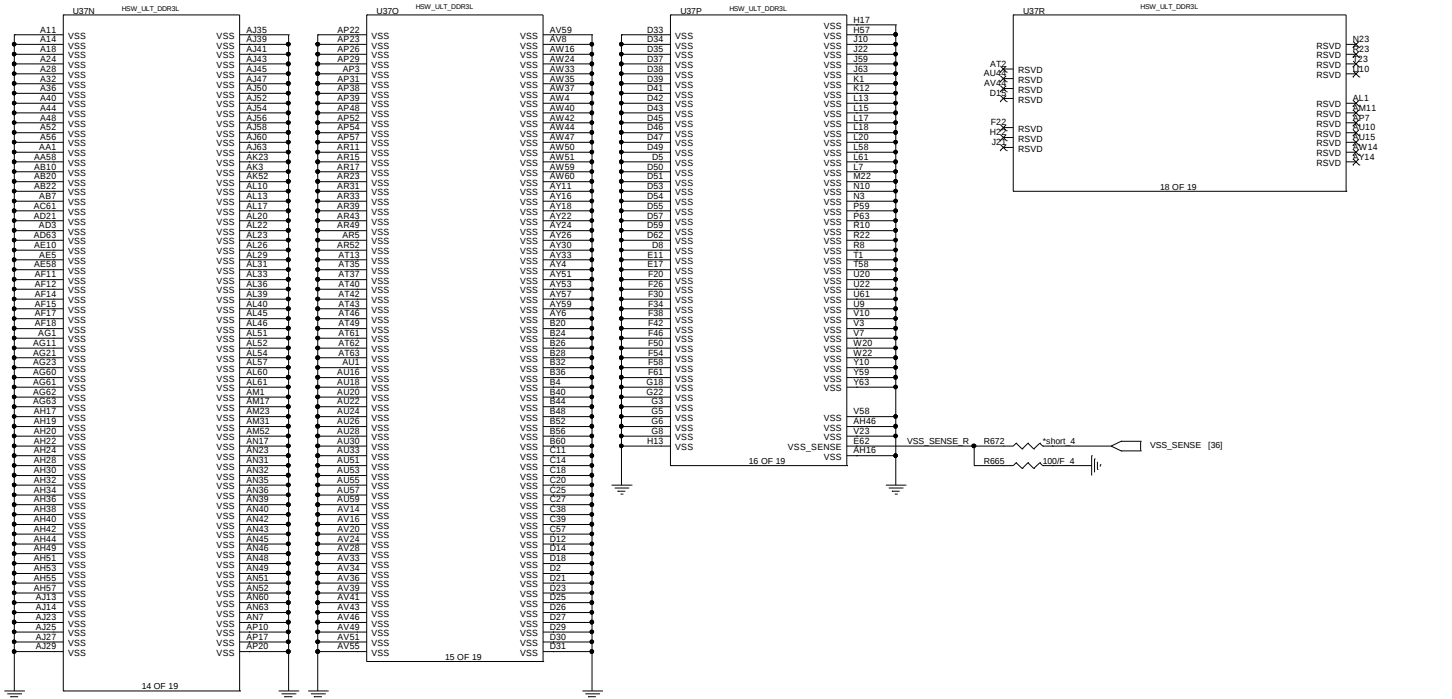
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)



Haswell ULT PCH (Power)



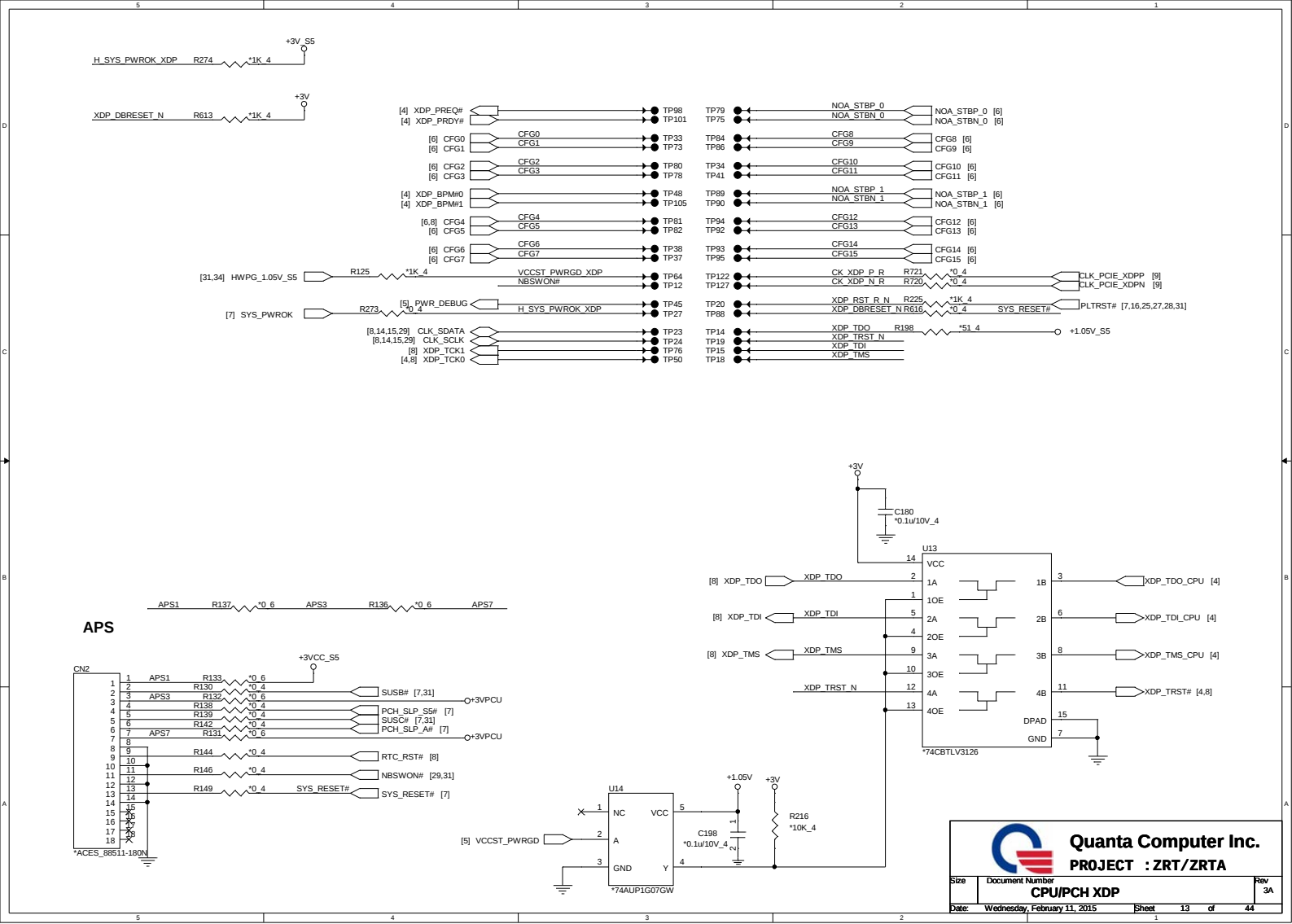
Haswell ULT (GND)

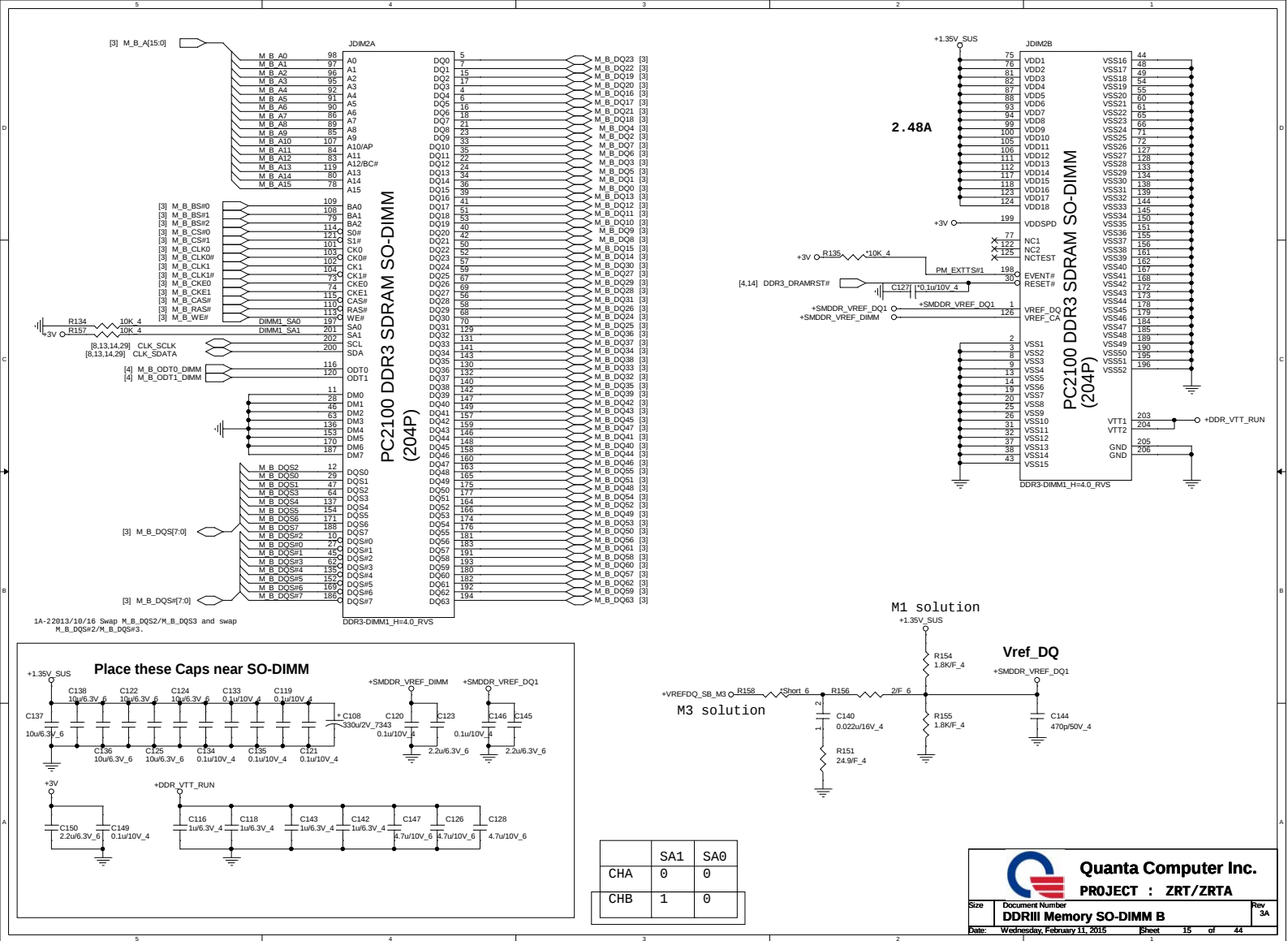




Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	LPT 6/6 (GND)	3A
Date	Wednesday, February 11, 2016	Sheet 12 of 44





PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL HVDD +
PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

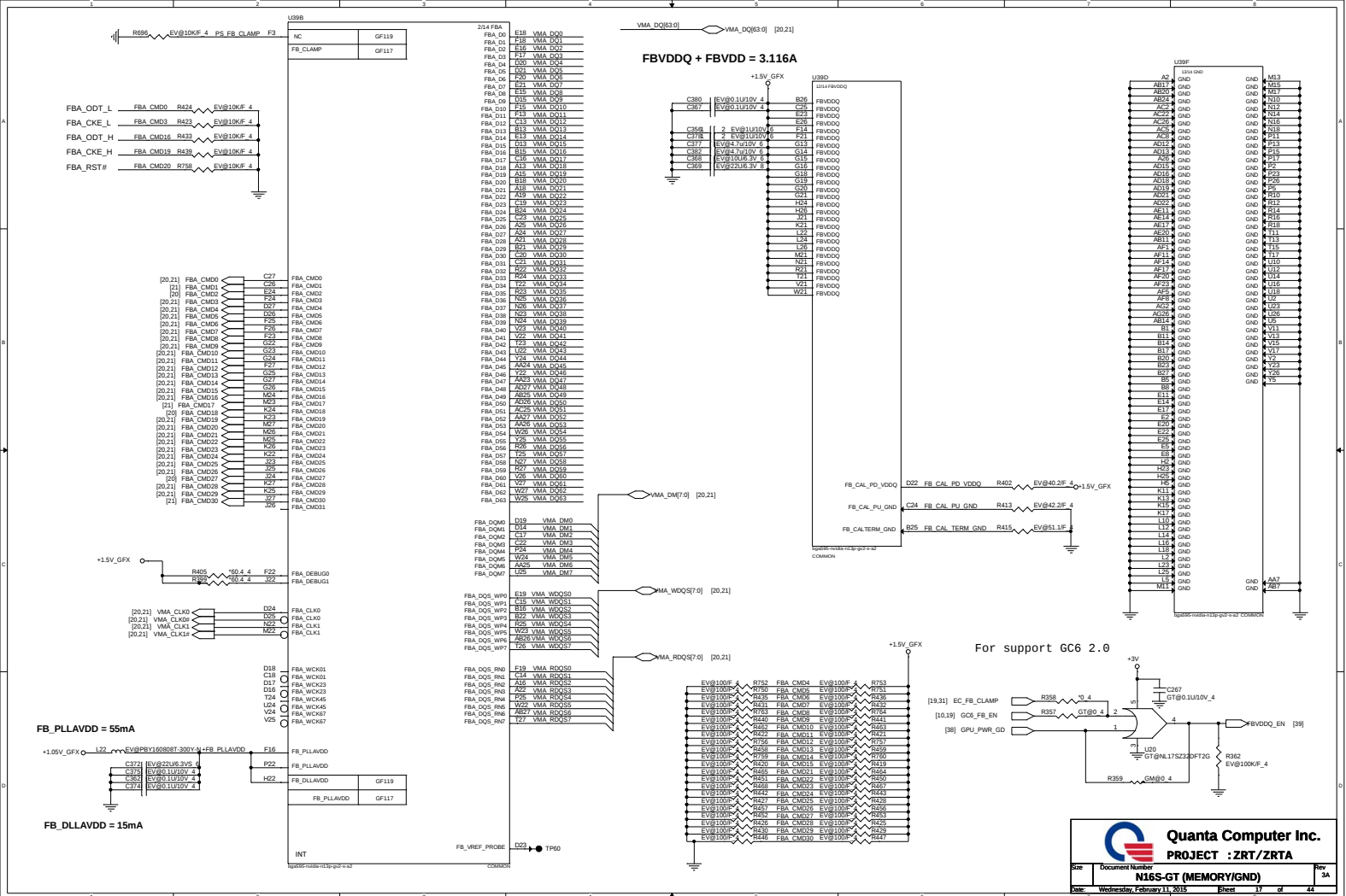
VDD33 = 56mA

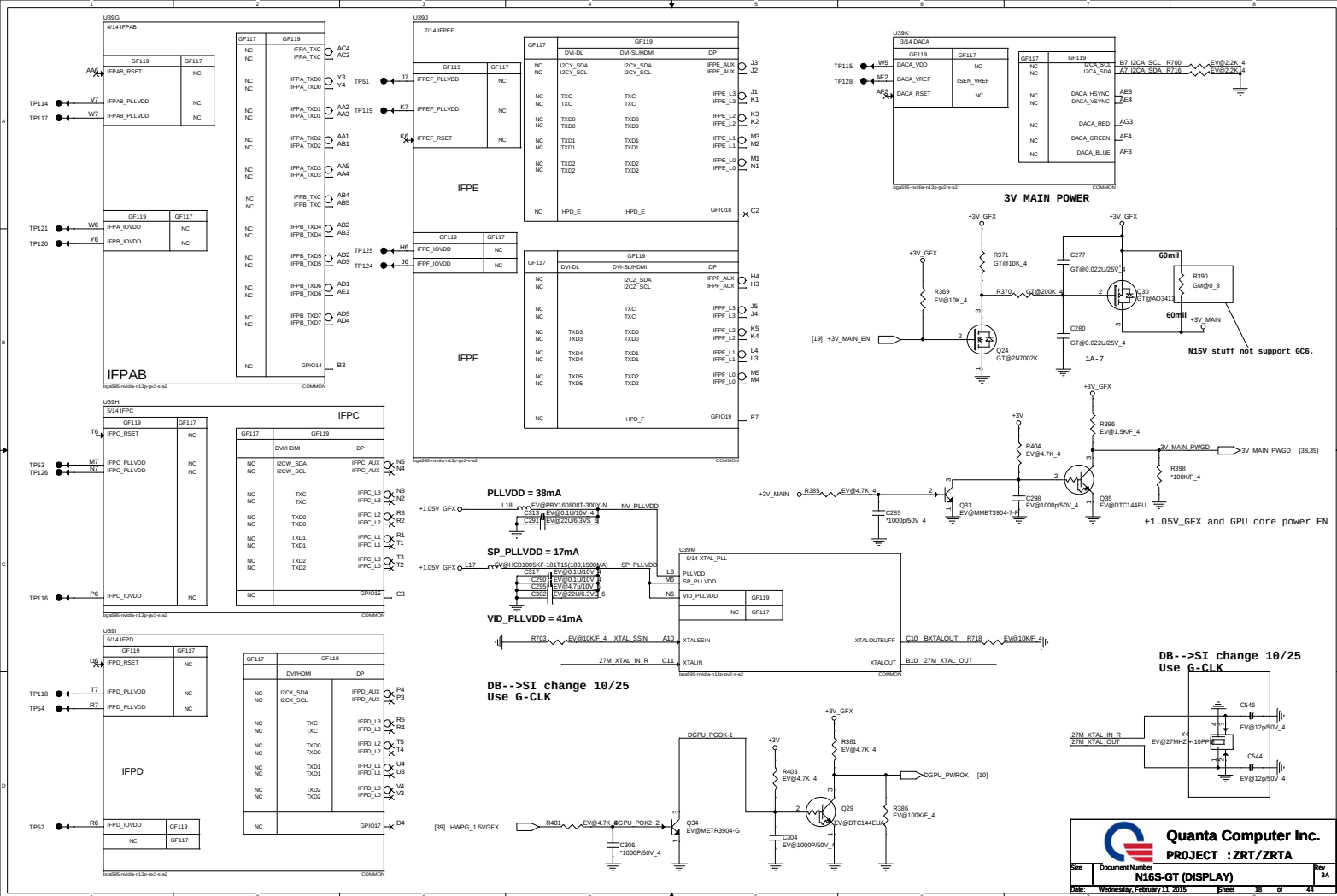
Power up
sequence

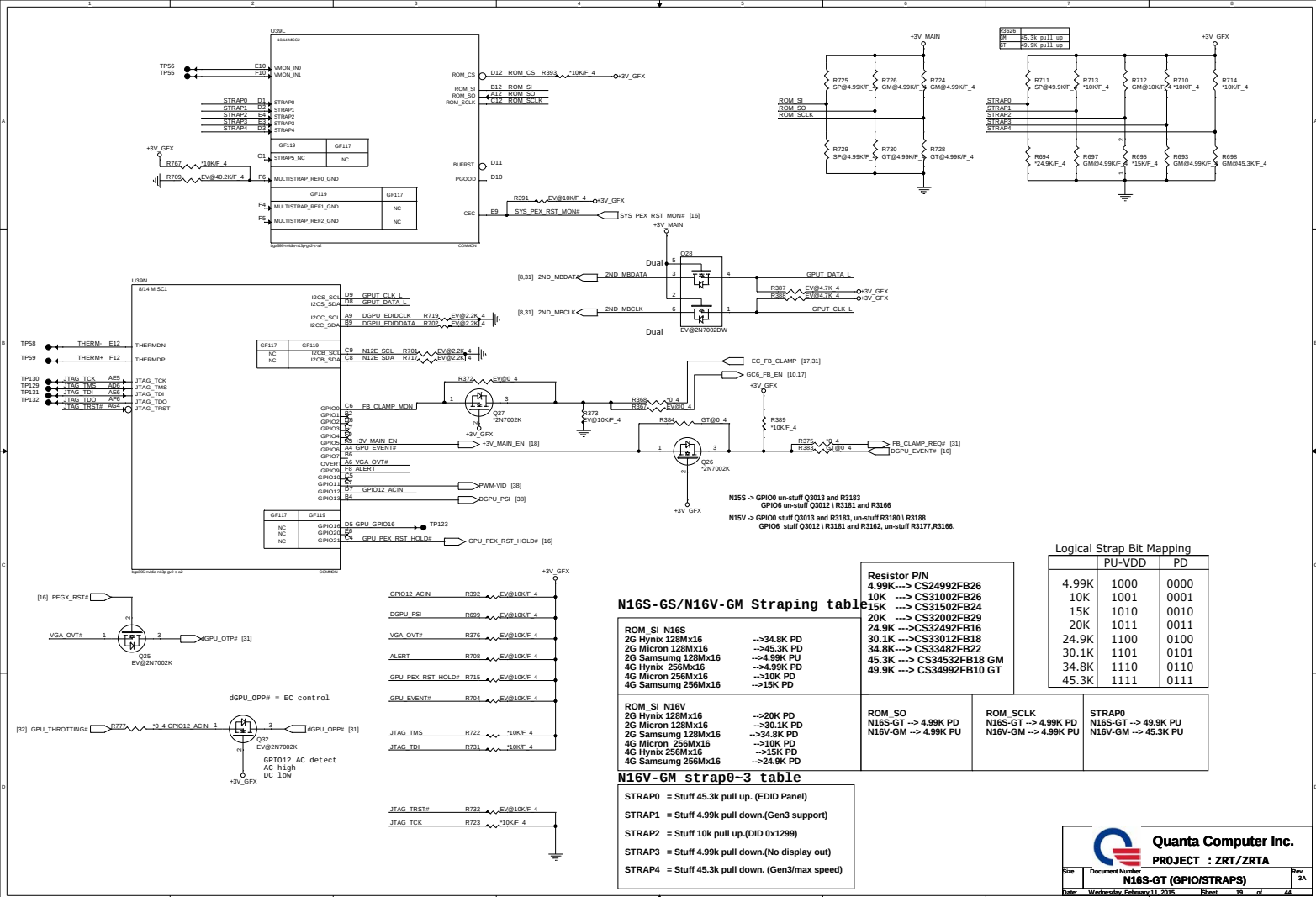
Power down
sequence

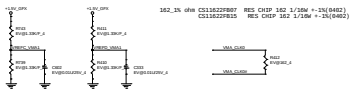
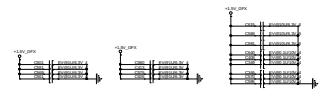
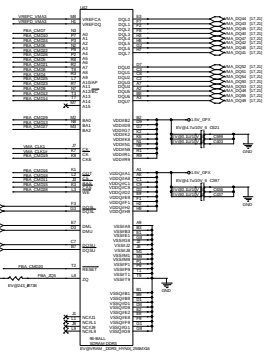
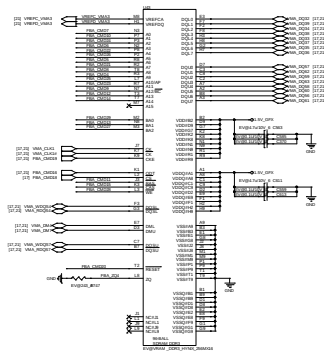
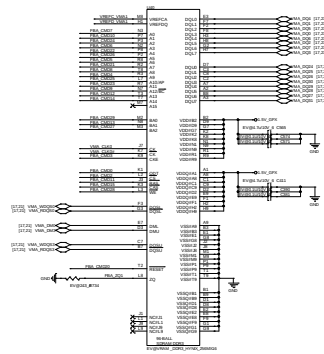
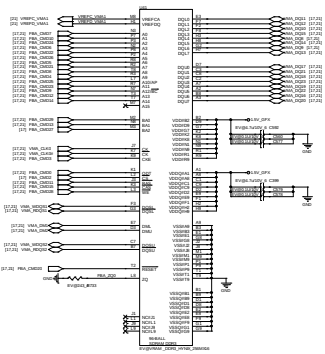
Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size Document Number
N16S-GT (PCIe IF) NVDD
Date: Wednesday, February 11, 2015
Rev 3A

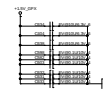
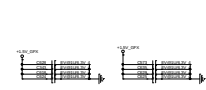


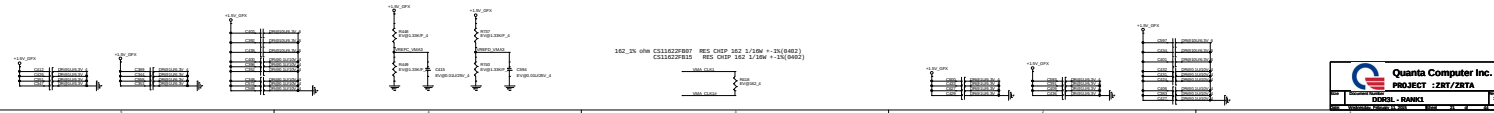
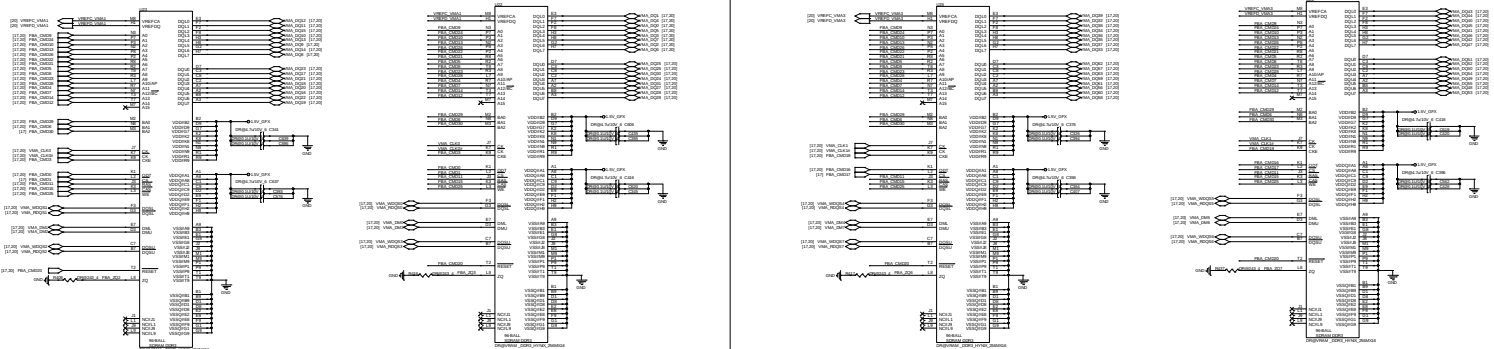




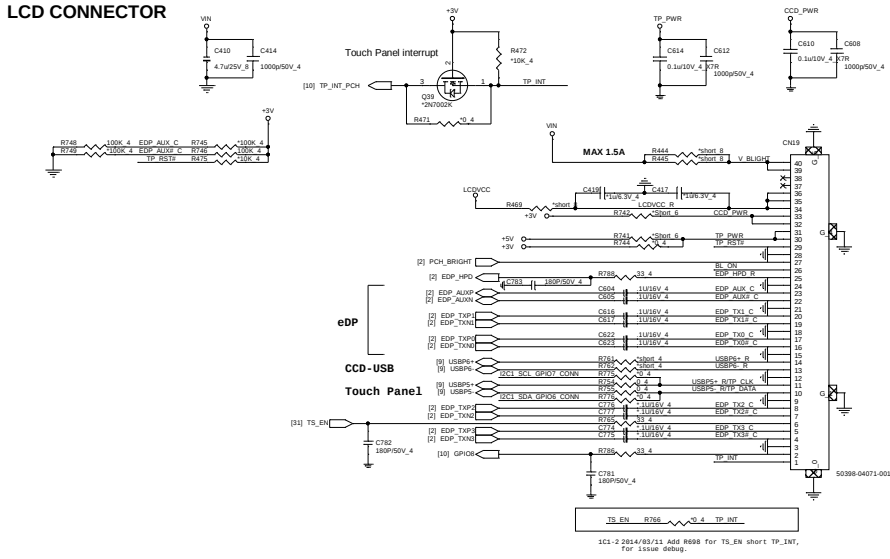


FOR EMI Request

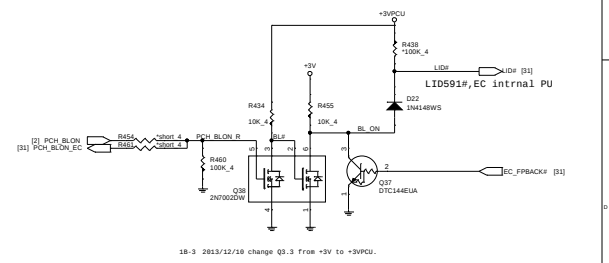






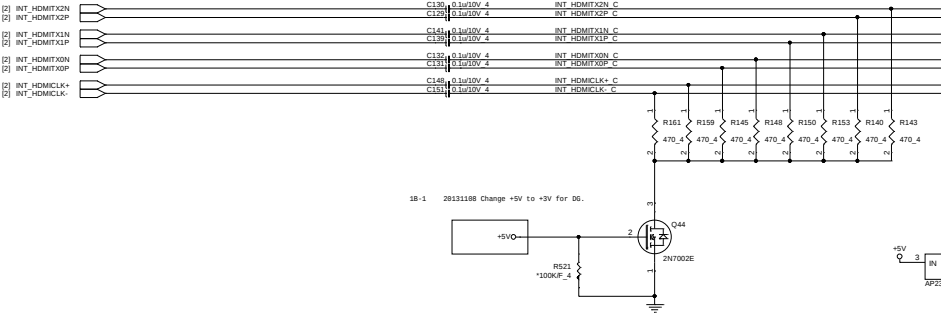
[illegible][illegible]

TPD>100KHz, TS=400kHz
Intel design guide suggestion
PCF 100 Pin 30U:
Per inch 3u TS=3x5inch
400kHz@100u s: 2.4~0.4k.
100KHz 10~100u9K~1k.

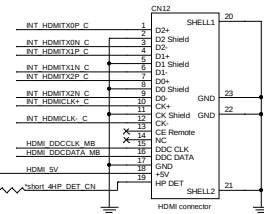
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HDMI

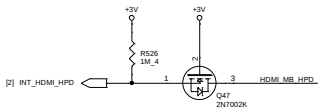
From PCH



HDMI connector



HDMI-detect

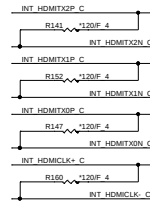


I2C

From PCH



EMI



Power trace tracking

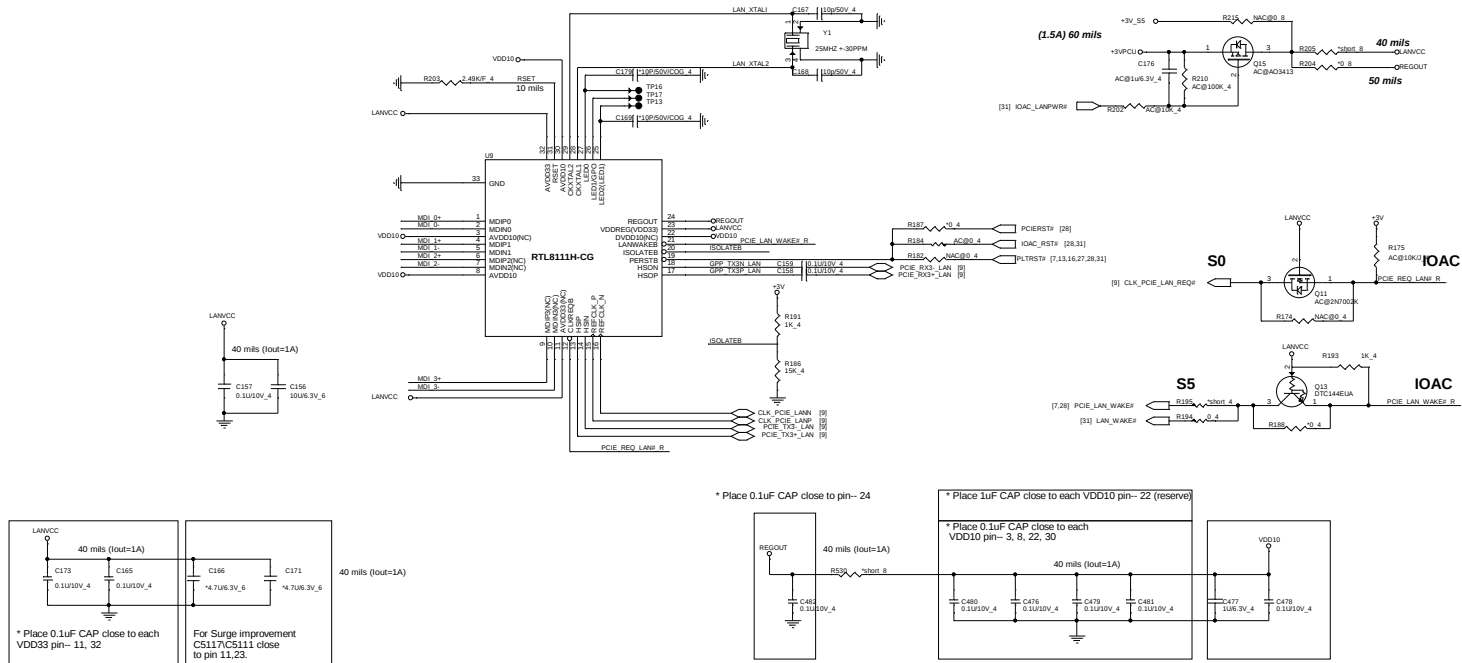
[2,5,7,8,9,10,11,12,14,15,16,17,18,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[23,23,26,27,29,33,37] +5V



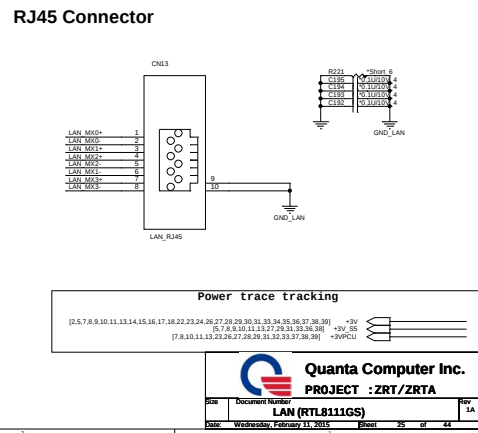
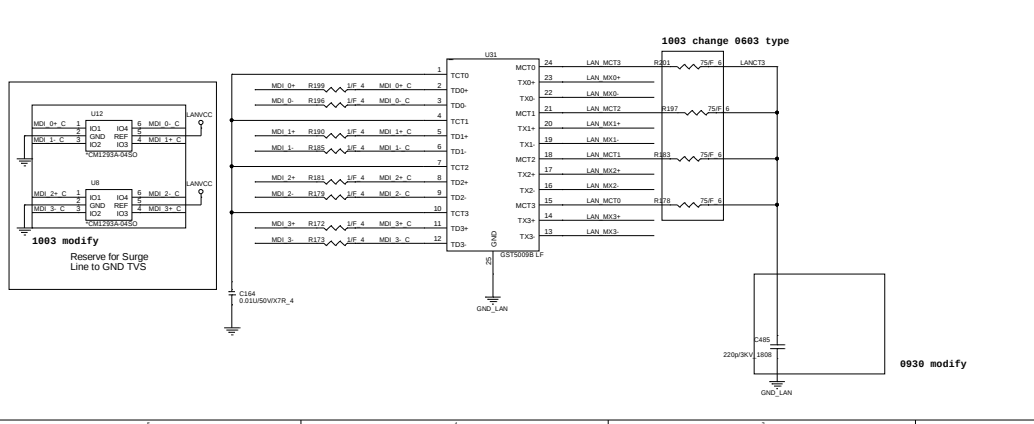
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
HDMI (P8101)

Size	Document Number	Rev
1A		1A

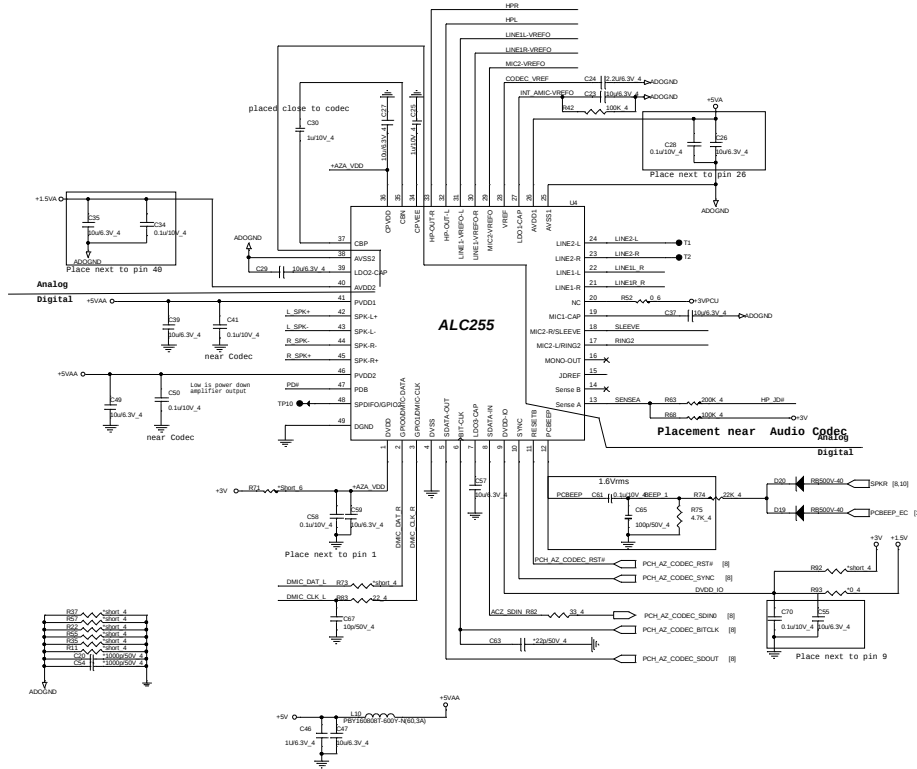
LAN



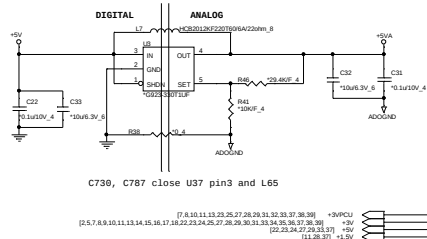
Transformer



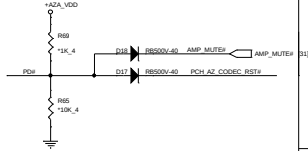
Codec(ADO)



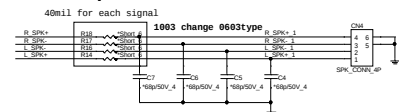
Codec PWR 5V(ADO)



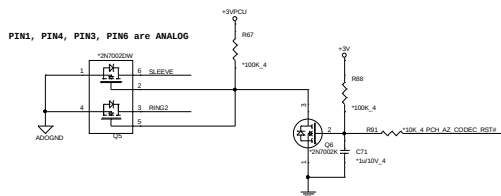
Mute(ADO)



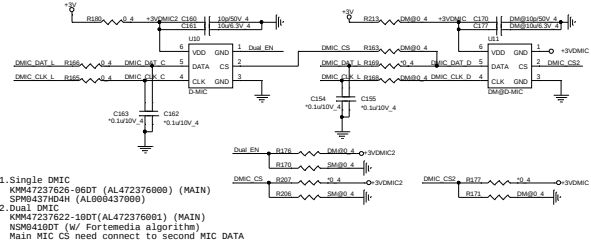
Internal Speaker



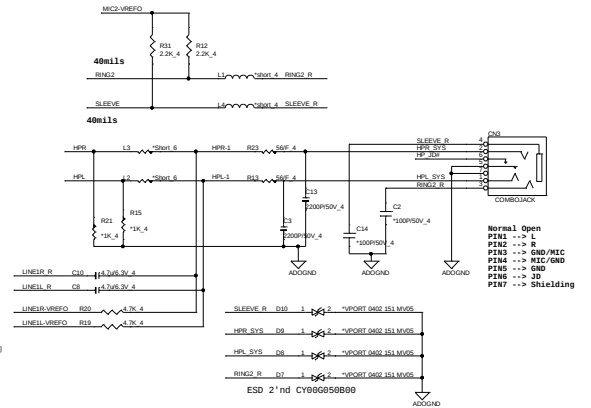
Grounding circuit(ADO)



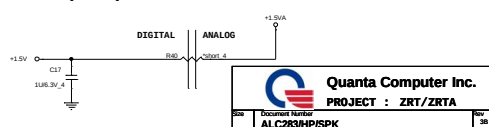
D-Mic



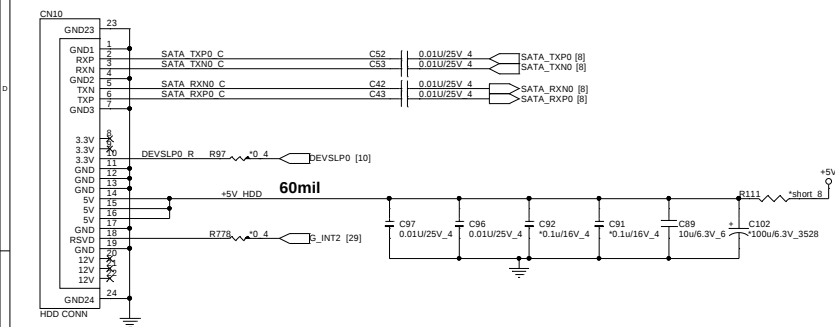
Universal Audio Jack



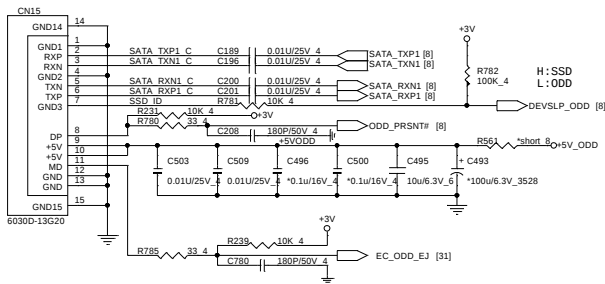
Codec PWR 3V/1.5V(ADO)



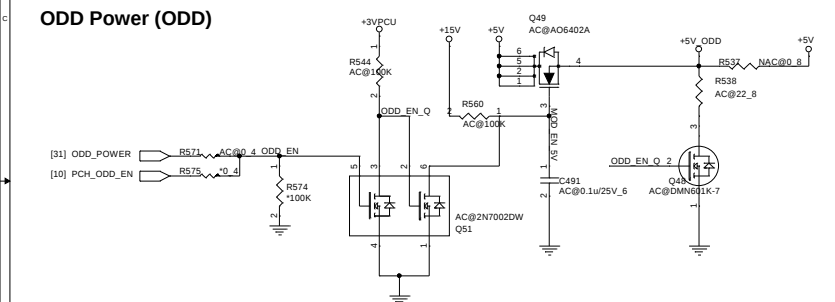
2.5" SATA HDD (HDD)



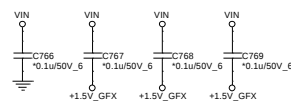
SATA ODD Connector(ODD)



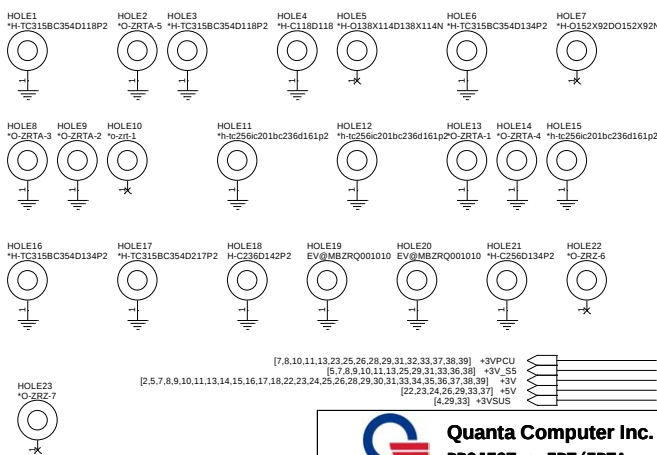
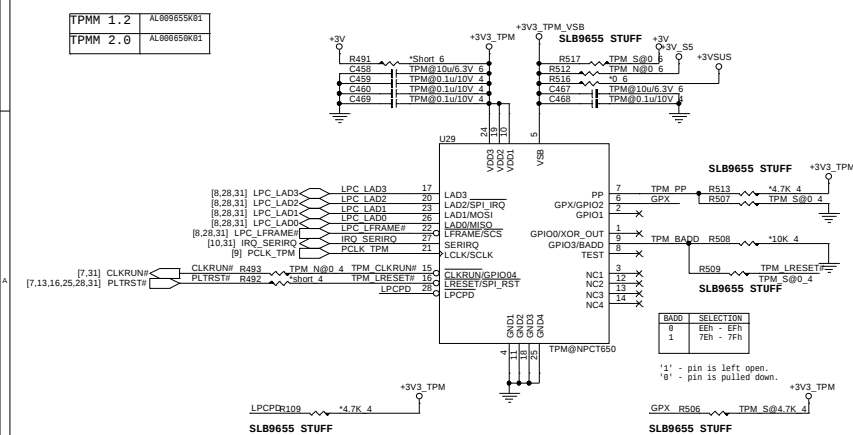
ODD Power (ODD)



EMI

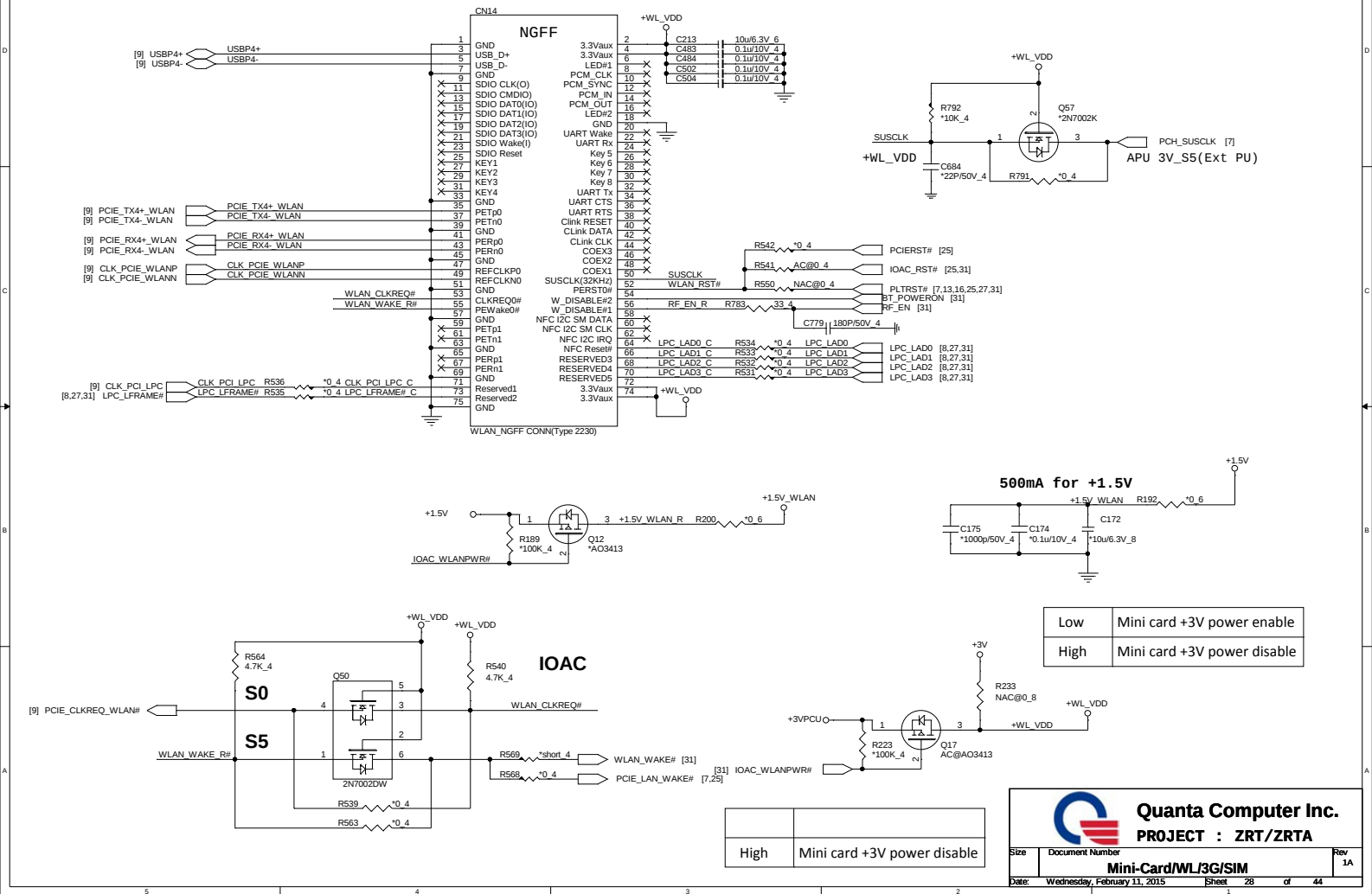


TPM NPCT650 (TPM)

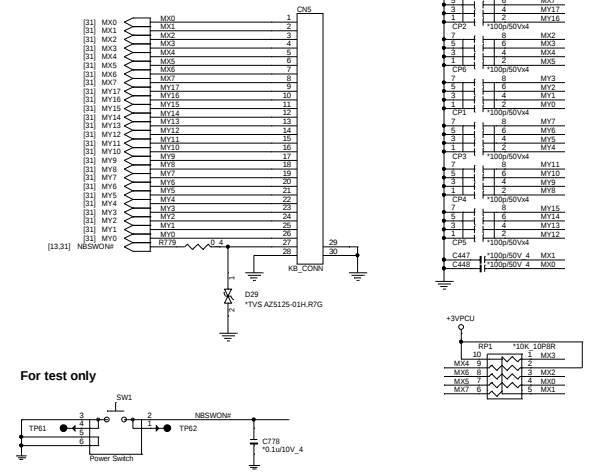


NGFF WiFi & BT (NGF)

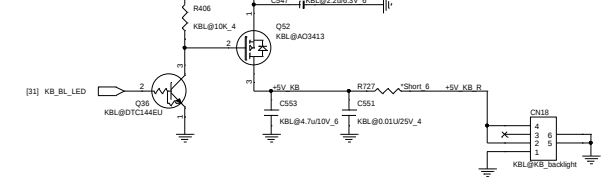
[7,8,10,11,13,23,25,26,27,29,31,32,33,37,38,39] +3VPCU [11,26,37] +1.5V [2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,27,29,30,31,33,34,35,36,37,38,39] +3V



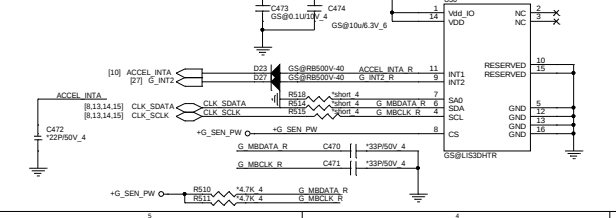
K/B (KBC)



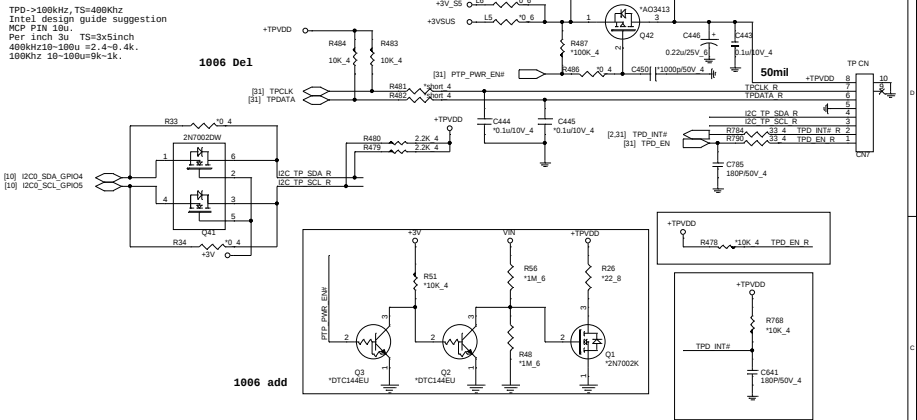
KB_BL LED (KBL)



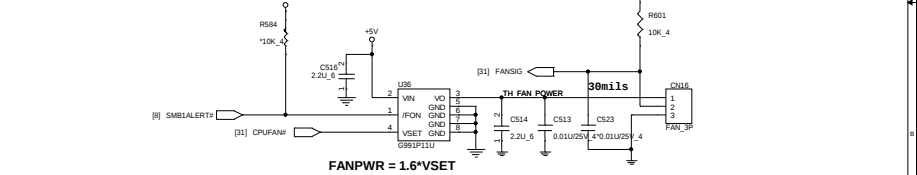
G-sensor(ACS)



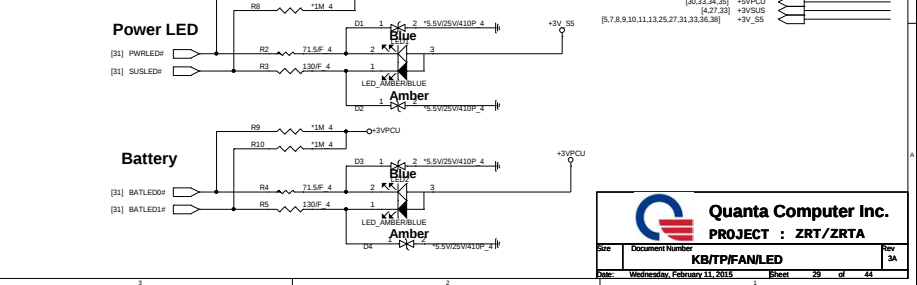
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



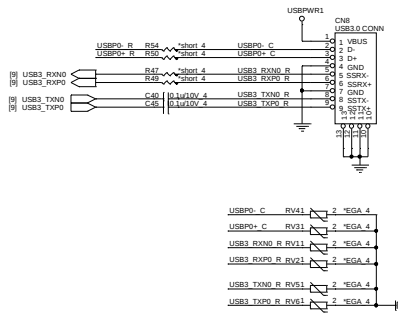
CPU FAN (THM)



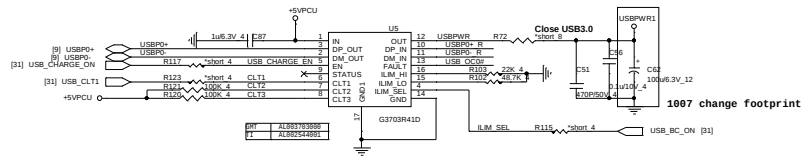
POWER LED(UIF)



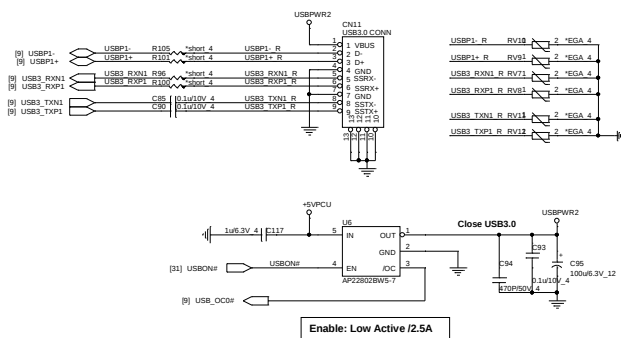
USB 3.0 Connector(UB3)



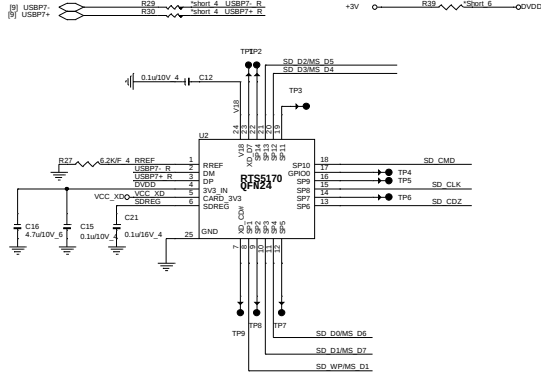
USB Charger for USB3.0 Port0 (UBC)



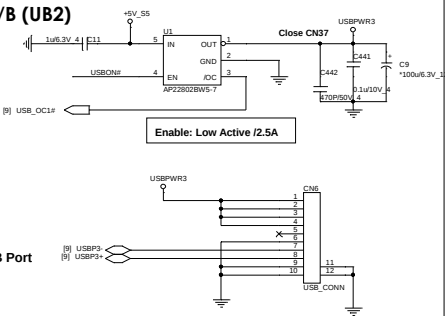
USB 3.0 Connector(UB3)



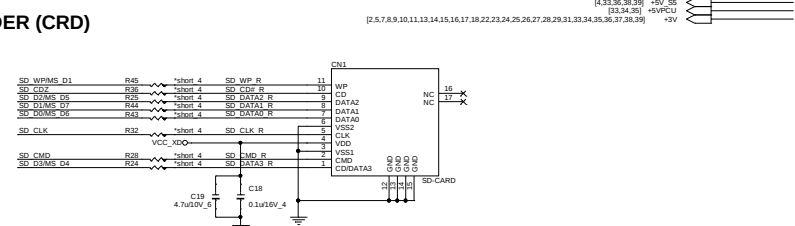
Card Reader (CRD)



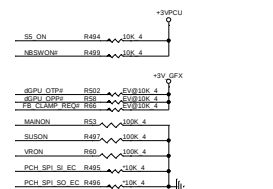
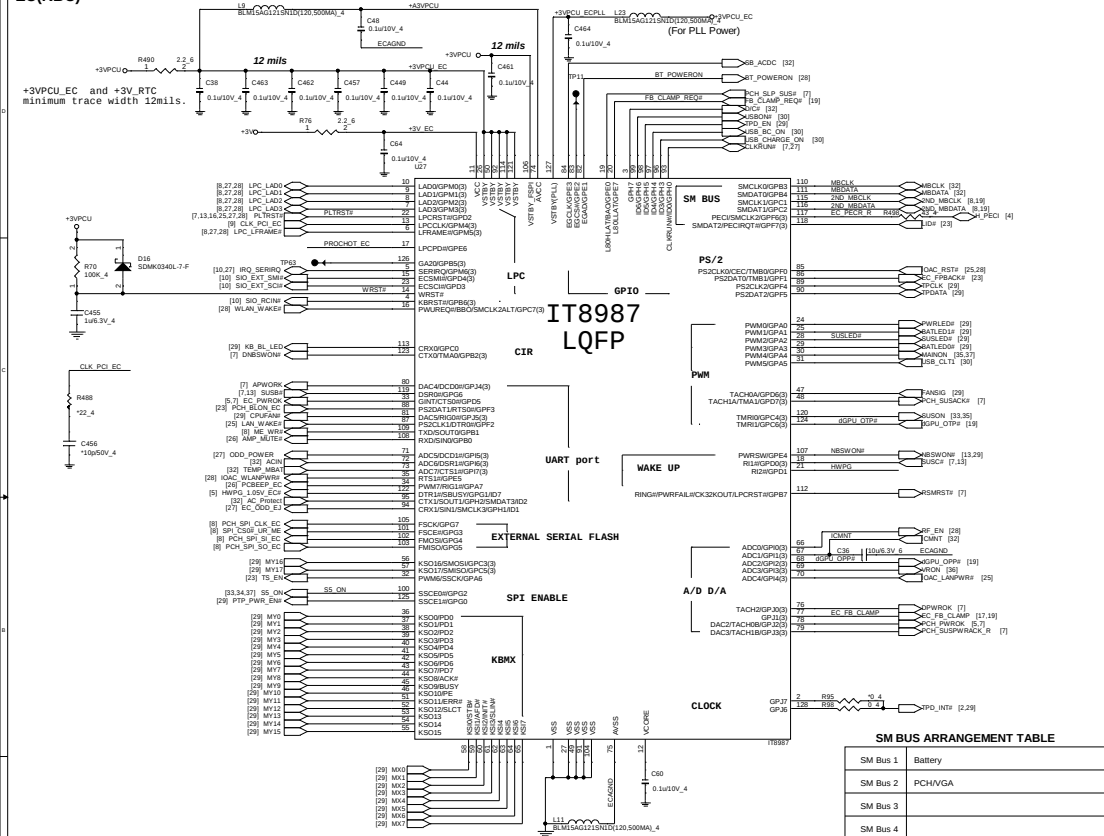
USB IO D/B (UB2)



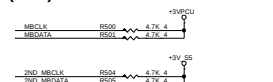
SD/MMC CARD READER (CRD)



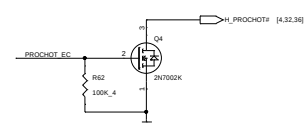
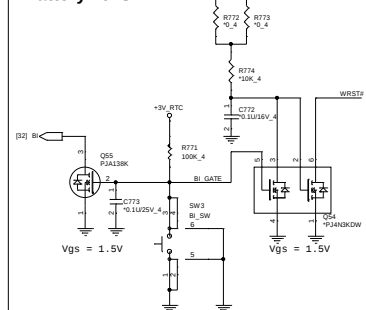
EC(KBC)



SM BUS PU(KBC)

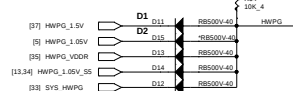


Battery B/I SW

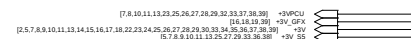


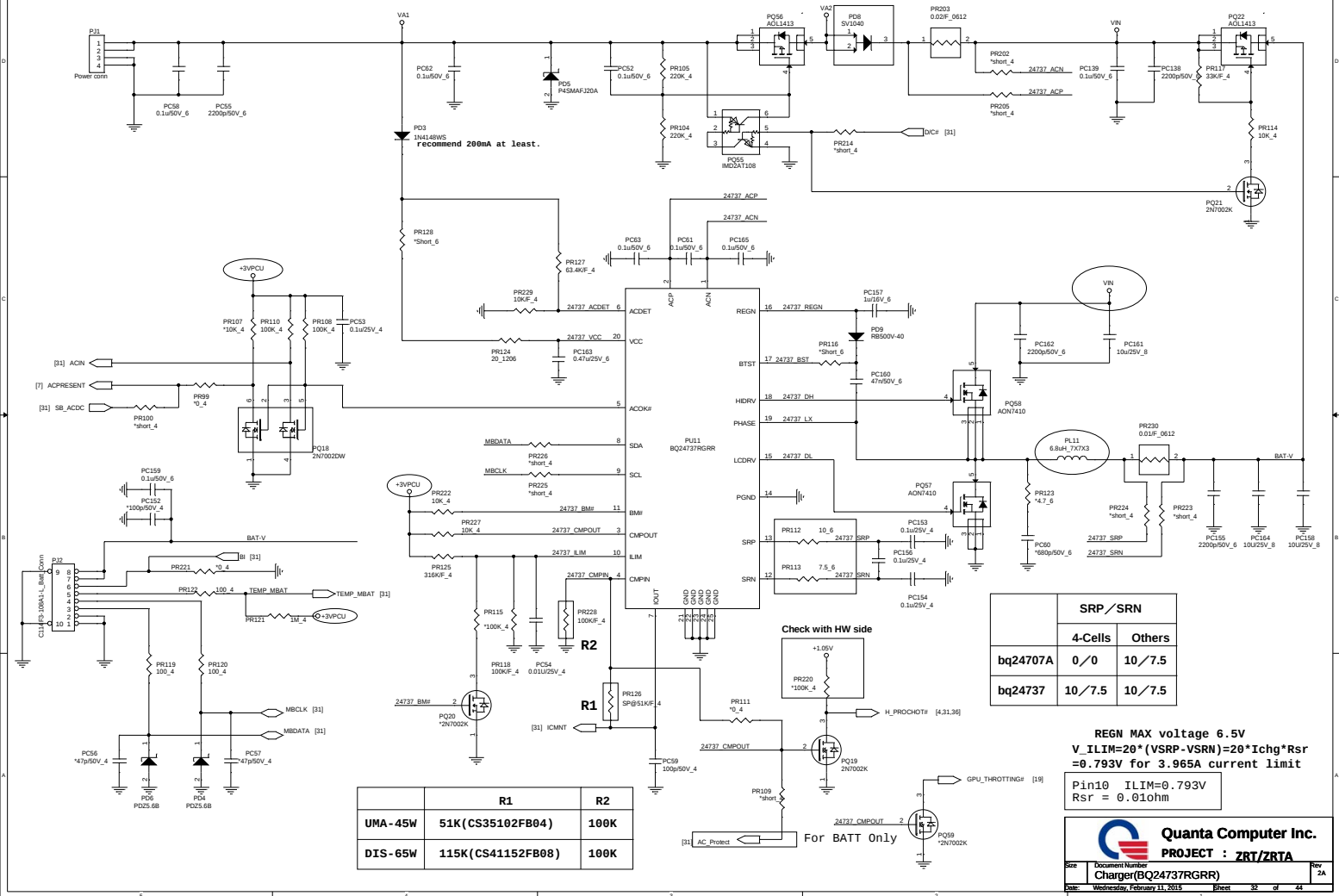
HWPG(KBC)

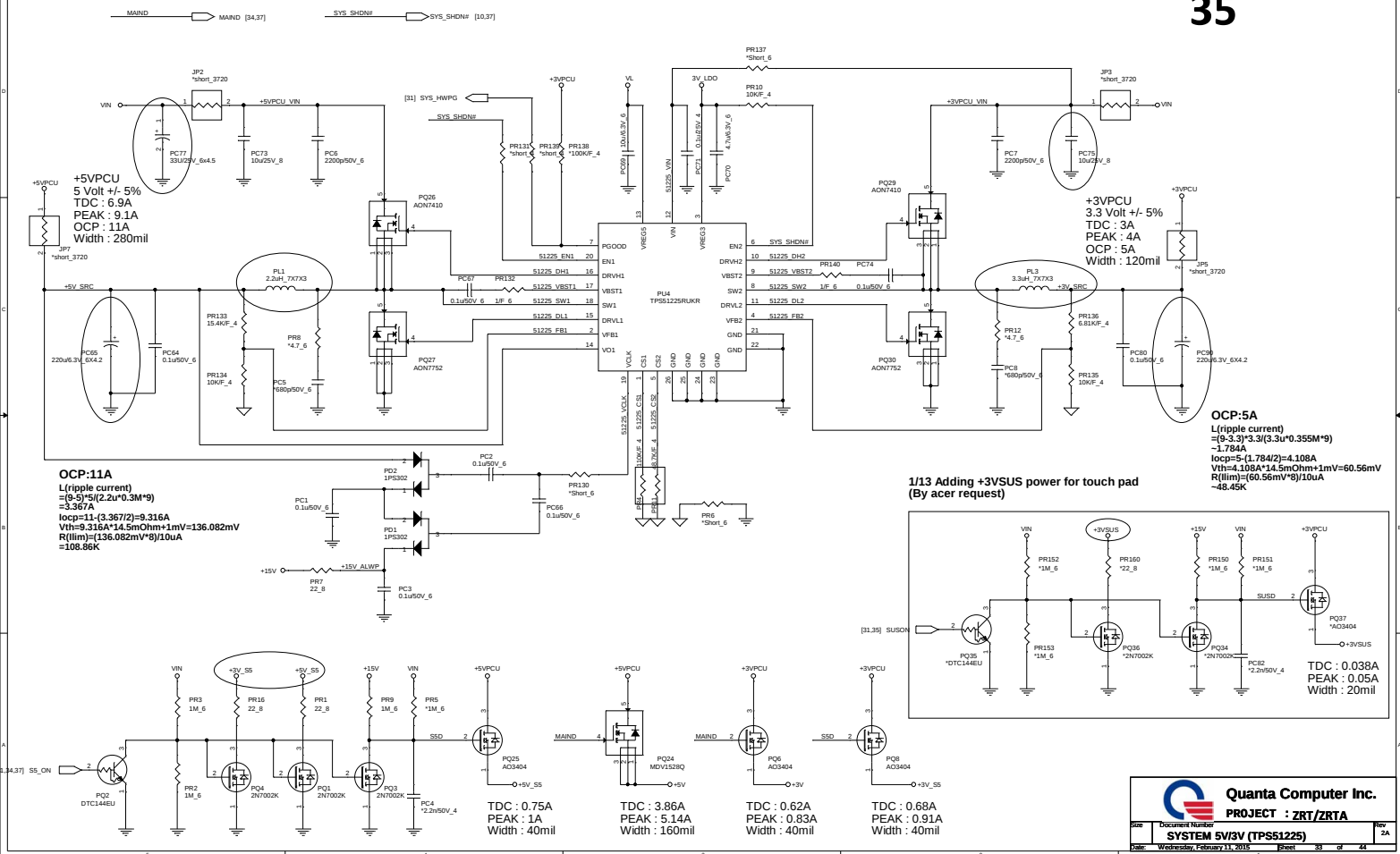
DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

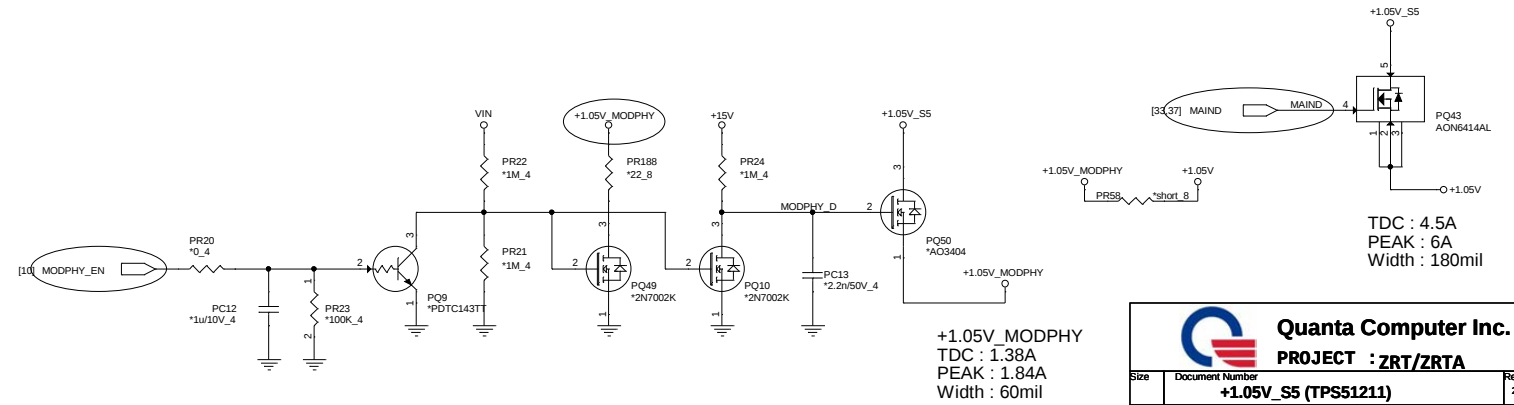
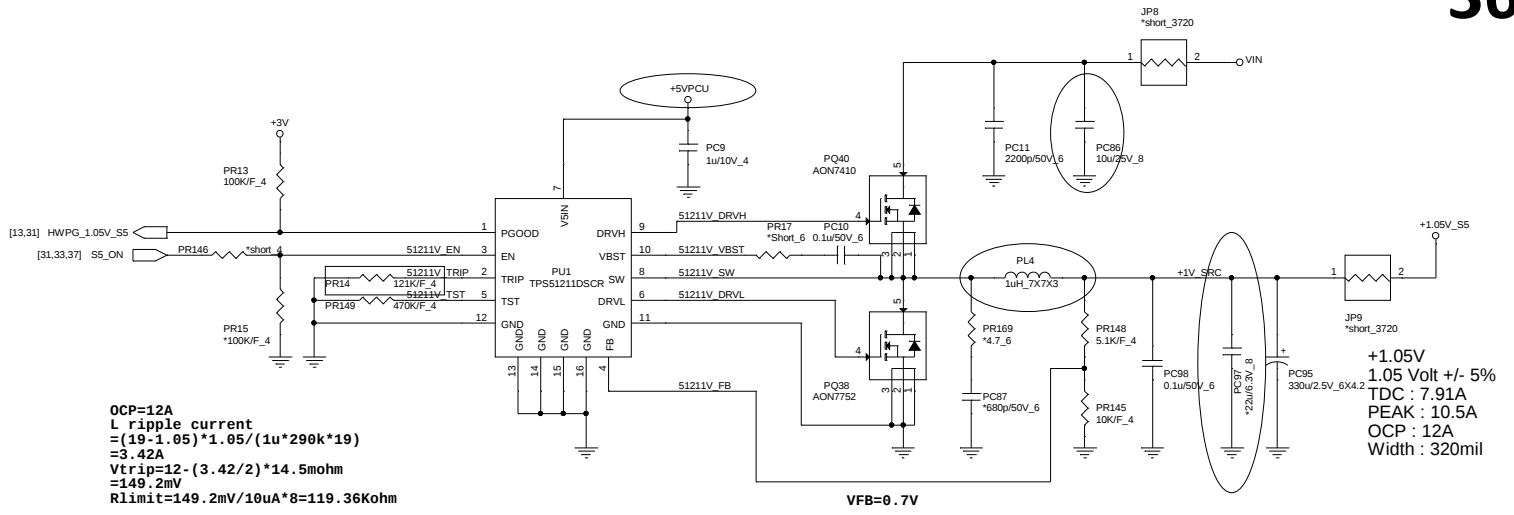
SM BUS ARRANGEMENT TABLE

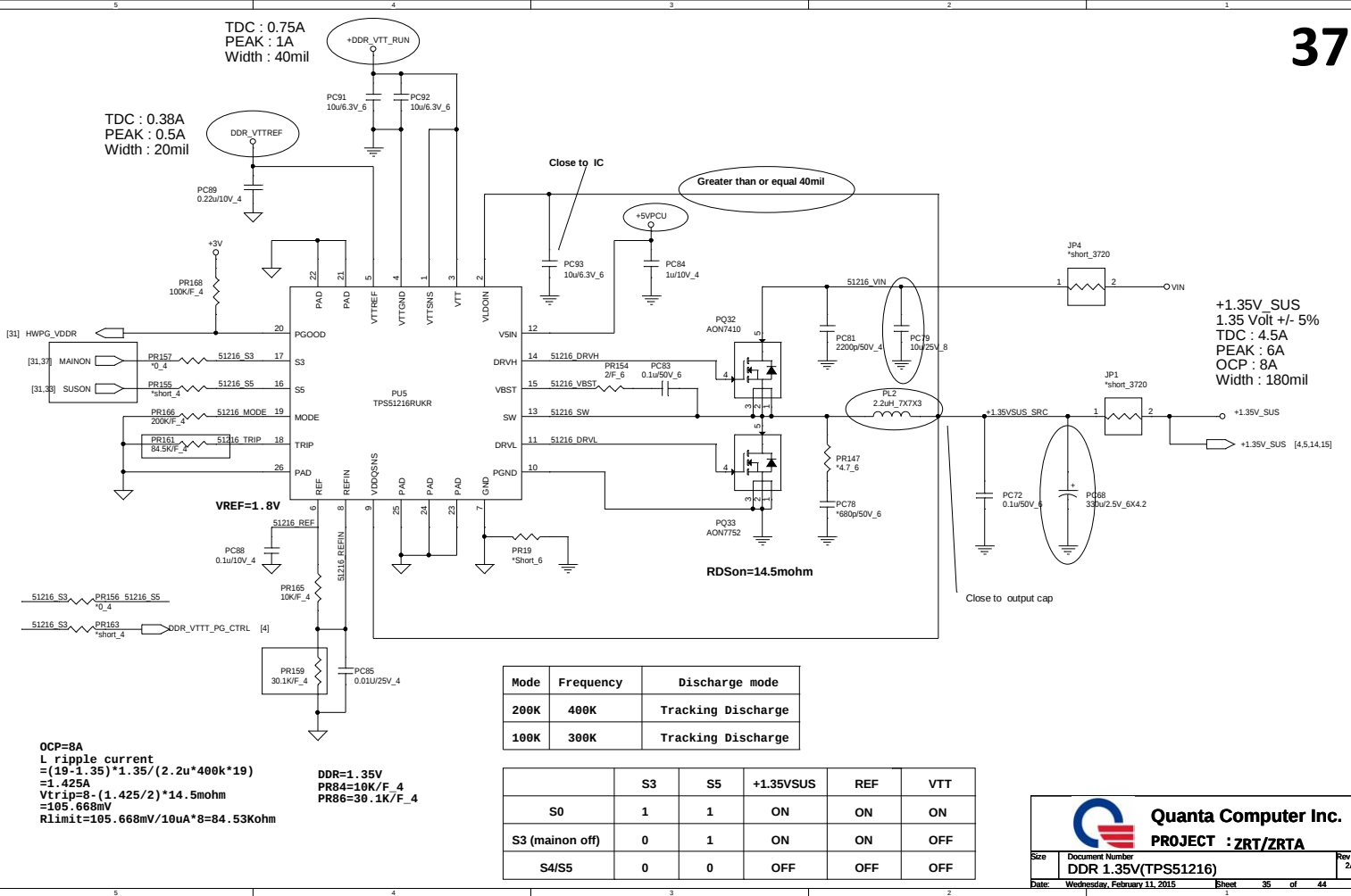
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

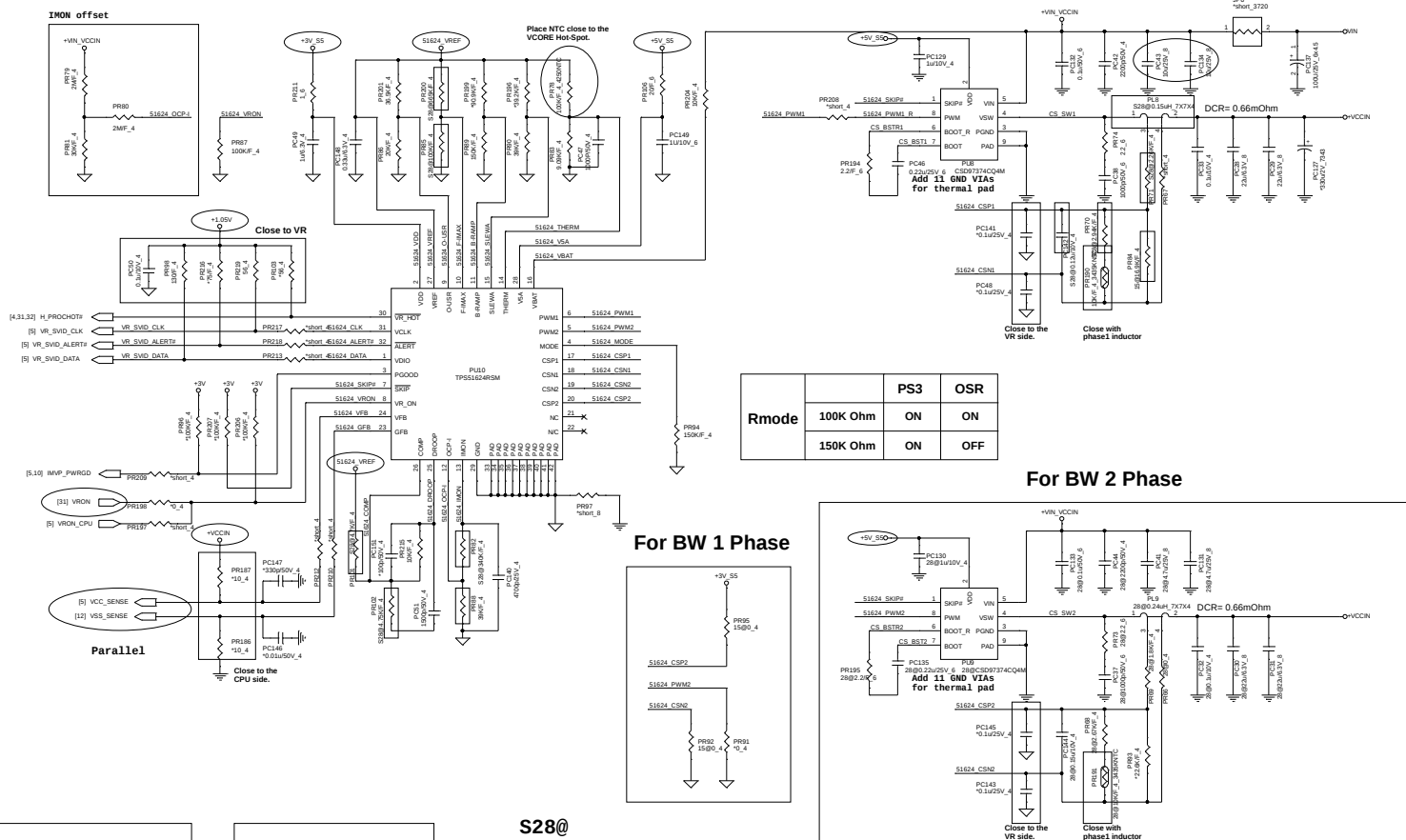


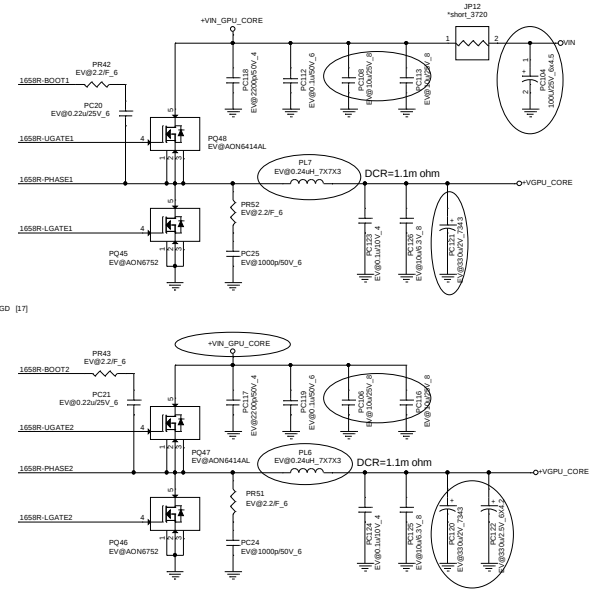






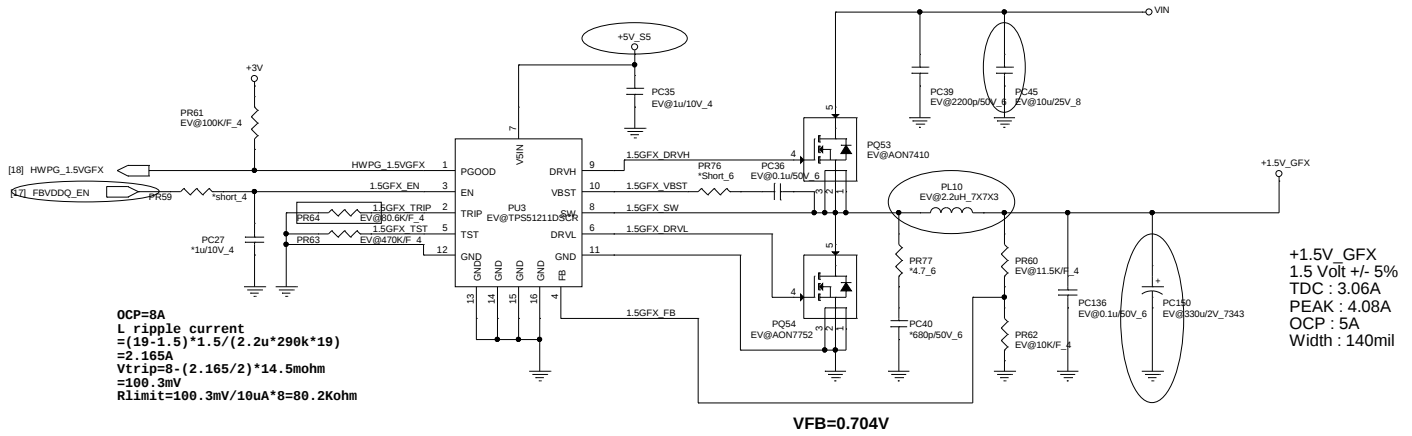
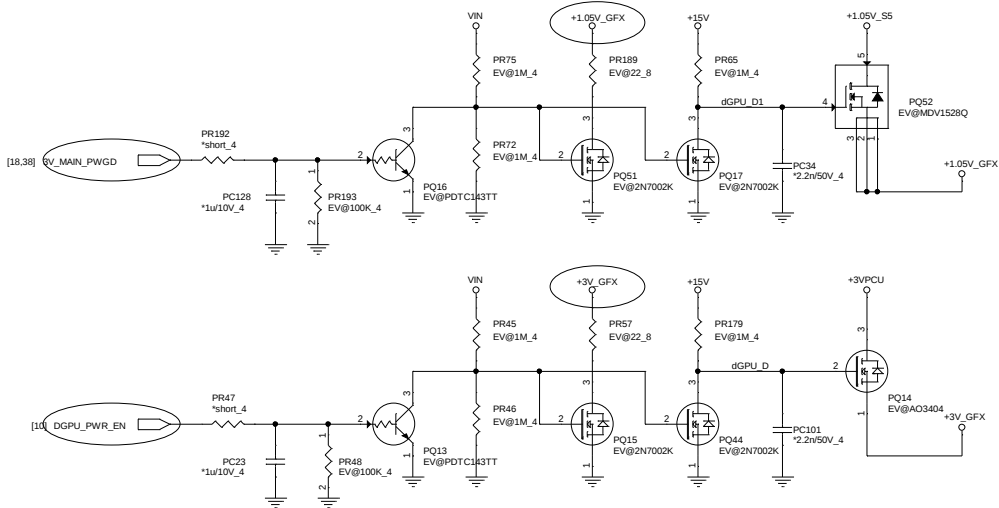






+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:A
FSW:300KHz
L/L=0mV/A

[16,17,18] +1.05V_GFX
[17,20,21,27] +1.5V_GFX
[16,18,19,31] +3V_GFX



OCP=8A
L ripple current

$$= (19-1.5) \times 1.5 / (2.2 \times 290 \times 19)$$

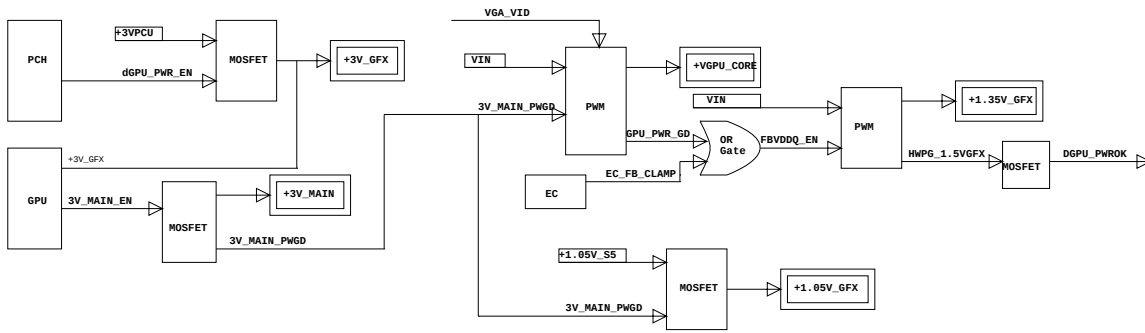
$$= 2.165A$$

$$V_{trip} = 8 - (2.165/2) \times 14.5 \text{mohm}$$

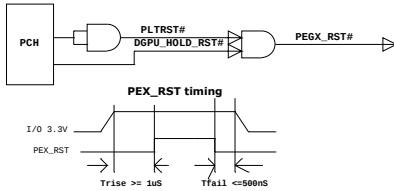
$$= 190.3 \text{mV}$$

$$R_{limit} = 190.3 \text{mV} / 10 \mu A \times 8 = 80.2 \text{Kohm}$$

VGA power up sequence



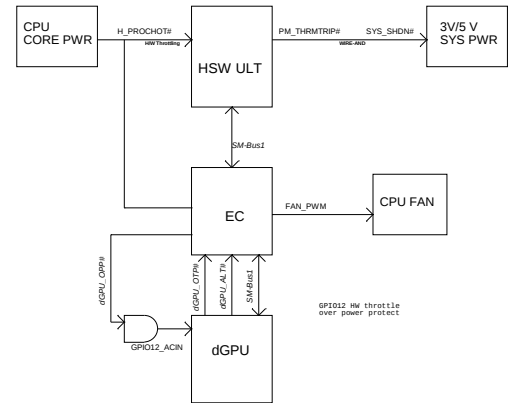
VGA Reset



Power States

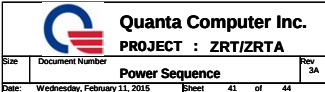
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V→+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V→+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAMBT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5VH	+5V	HDD/SPKHDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GFX/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+3V_GFX	variation	DGPAU GPU POWER	DGPAU_PWR_EN	S0
+1.05V_GFX	+3.3V	External GPU POWER	3V_MAIN_EN	S0
+VGPU_CORE	+1.35V	External GPU POWER	3V_MAIN_EN	S0
+1.35V_GFX	+1.05V	External GPU POWER	FBVDDQ_EN	S0

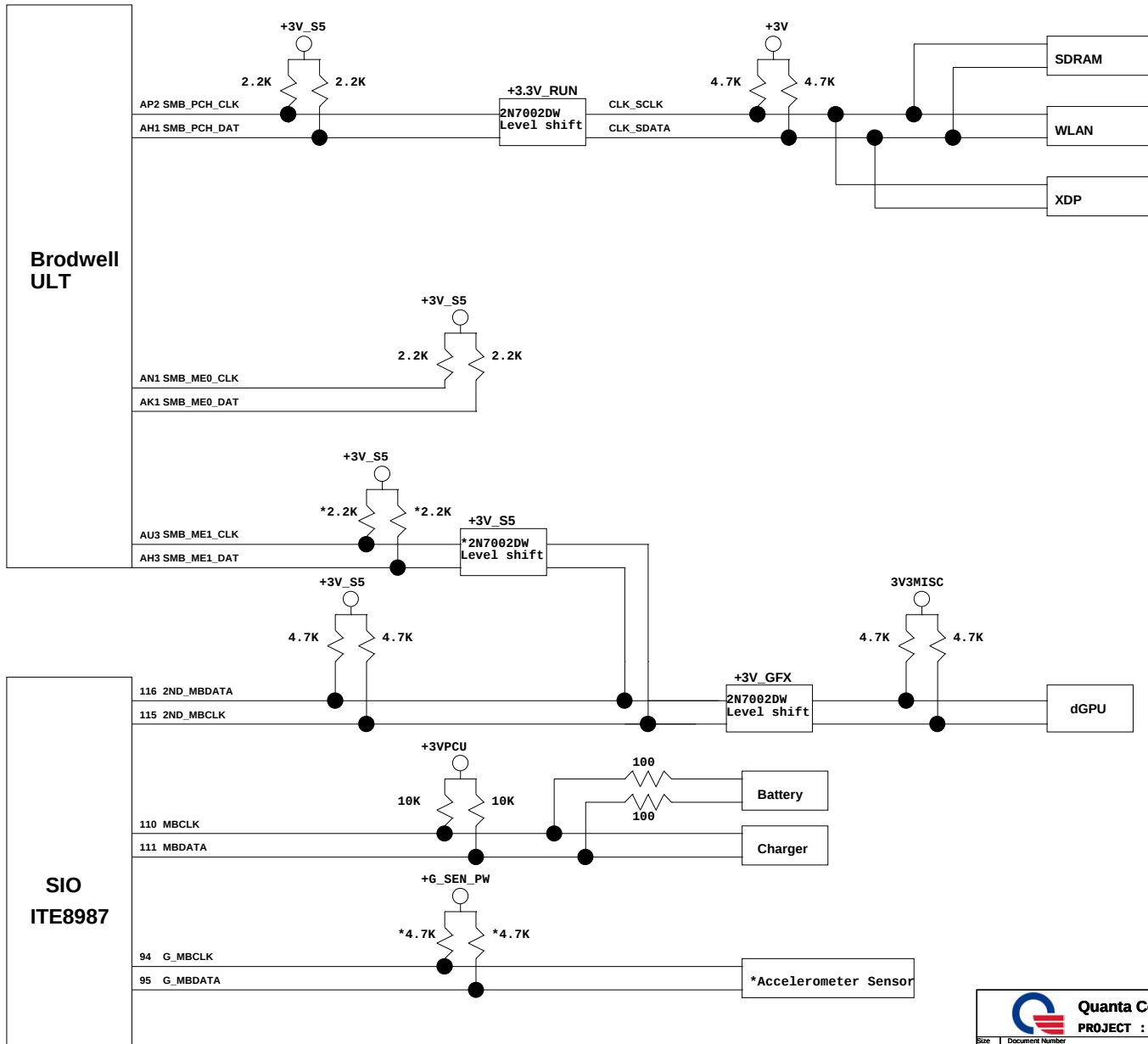
Thermal Follow Chart

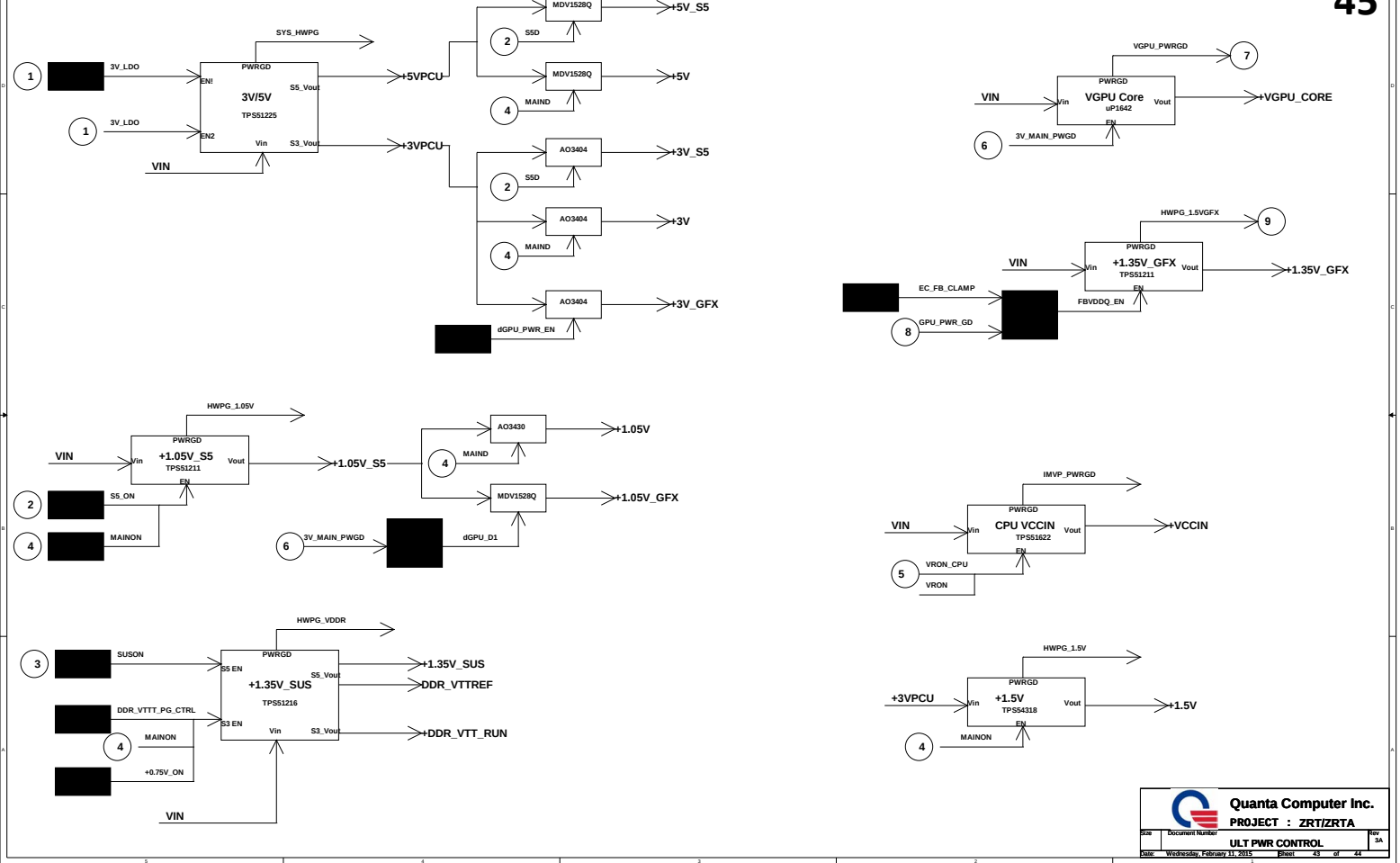


```
dGPU_OPP# EC notify HW throttle over power protect
dGPU_OTP# VGA thnatrip# => inform EC over temperature protect
```

40







[illegible]